STABILITY AND COMPENSATION

Stability and Compensation

- Ground Loops
- Supply Loops
- Local Internal Loops
- Coupling: Internal and External
- Aol Loop Stability

Eliminate Coupling

Internal and External

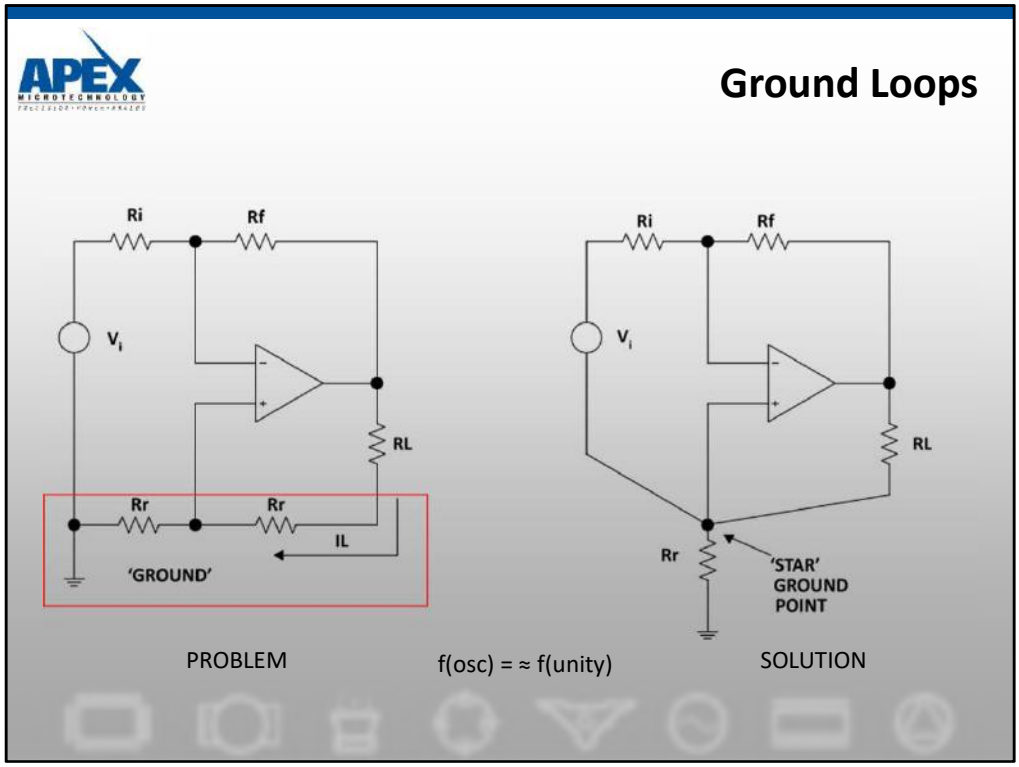
- Ground the Case
- Reduce Impedances
- Eliminate I_b Compensation Resistor on +IN
- Don't Run Output Traces Near Input Traces
- Run I_{out} Traces Adjacent to I_{out} Return Traces

1. Grounding the case forms a Faraday shield around the internal circuitry of the power amplifier which prevents unwanted coupling from external noise sources.
2. Reducing impedances keeps node impedances low to prevent pick-up of stray noise signals which have sufficient energy only to drive high impedance nodes.
3. Elimination of the Ib compensation resistor on the +input will prevent a high impedance node on the +input which can act as an antenna, receiving unwanted noise or positive feedback, which would result in oscillations. This famous Ib compensation resistor is the one from the +input to ground when running an amplifier in an inverting gain. The purpose of this resistor is to reduce input offset voltage errors due to bias current drops across the equivalent impedance as seen by the inverting and non-inverting input nodes. Modern op amps feature compensated input stages and benefit very little from this technique.

Calculate your DC errors without the resistor. Some op amps have input bias current cancellation negating the effect of this resistor. Some op amps have such low input bias currents that the error is insignificant when compared with the initial input offset voltage. Leave this +input bias resistor out and ground the +input if possible. If the resistor is required, bypass it with a 0.1µF capacitor to ground.

4. Don't route input traces near output traces. This will eliminate positive feedback through capacitive coupling of the output back to the input.
5. Run Iout traces adjacent to Iout return traces. If a printed circuit board has both a high current output trace and a return trace for that high current , then these traces should be routed adjacent to each other (on top of each other on a multi-layer printed circuit board) so they form an equivalent twisted pair by virtue of their layout. This will help cancel EMI generated from outside from feeding back into the amplifier circuit.

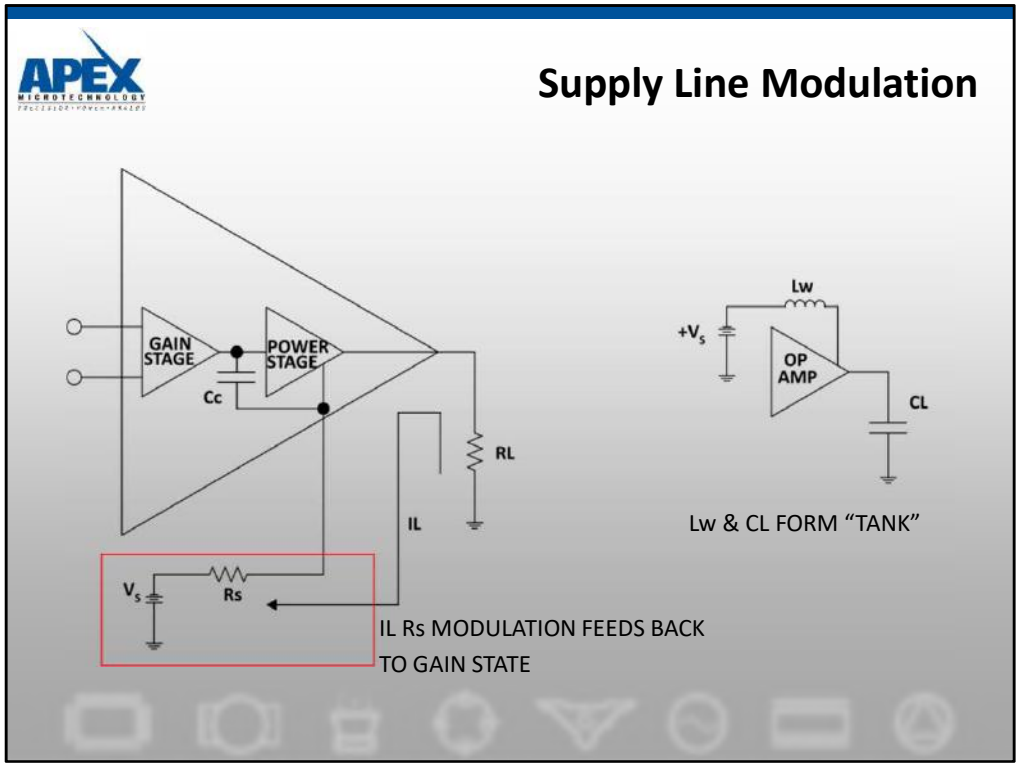
1. Ref. AN1 STABILITY, AN19



Ground loops come about from load current flowing through parasitic layout resistances, causing part of the output signal to be fed back to the input stage. If the phase of the signal is in phase with the signal at the node it is fed back to, it will result in positive feedback and oscillation. Although these parasitic resistances (Rr) in the load current return line cannot be eliminated, they can be made to appear as a common mode signal to the amplifier. This is done by the use of a star ground point approach.

The star point is merely a point that all grounds are referred to, it is a common point for load ground, amplifier ground, and signal ground. The star ground point needs to be a singular mechanical feature. Run each connection to it such that current from no other part of the circuit can mingle until reaching the star point. Don't forget your star point when making circuit measurements. Moving the ground lead around may change the indication leading to false assumptions about circuit operation.

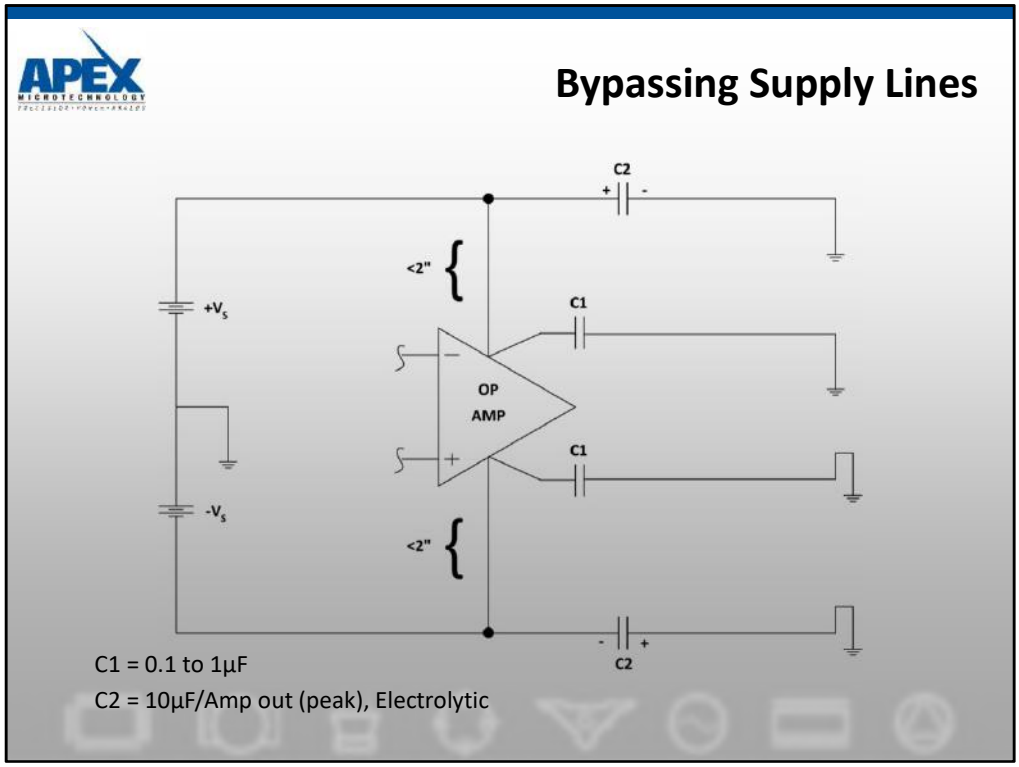
Ref. AN1 STABILITY, AN19



Supply loops are another source of oscillation. In one form of power supply related oscillations the load current flowing through supply source resistance and parasitic trace resistance modulates the supply voltage seen at the power supply pin of the op amp. This signal voltage is then coupled back into a gain stage via the compensation capacitor which is usually referred to one of the supply lines as an AC ground.

Another form of oscillatory circuit that can occur is due to parasitic power supply lead inductance reacting with load capacitance to form a high Q tank circuit.

Ref. AN1 STABILITY, AN19

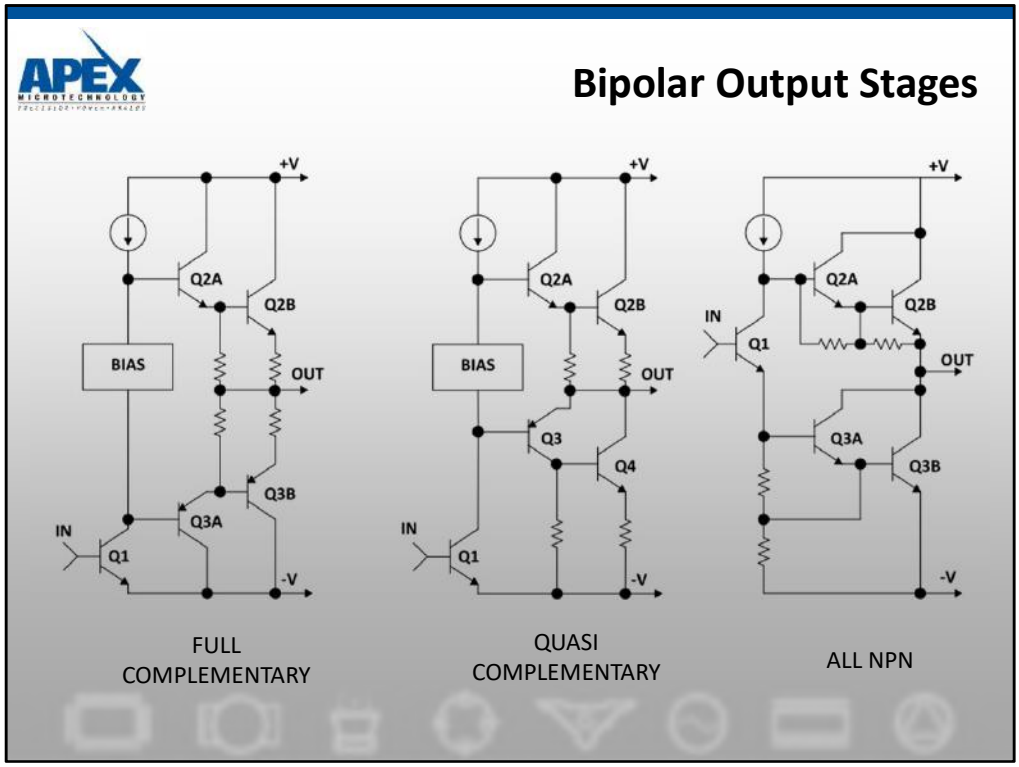


All supply line related oscillation and coupling problems can be avoided with proper bypassing.

The "must do" in all bypassing is a good high frequency capacitor right at each amplifier or socket power supply pin to ground. Not just any ground but the star point ground. This will most often be a multilayer ceramic, at least 1000pF, and as large as possible up to about 1µF. Above that capacitance high frequency characteristics shouldn't be taken for granted. Polysterene, polypropylene, and mylar are possible alternatives when ceramics cannot be used for any reason. Check the manufacturer's data sheet for low ESR at least two times the unity gain bandwidth of the op amp being used.

Once high frequency bypassing is addressed, additional low frequency decoupling is advisable. In general use about 10µF/amp of peak output current, either electrolytic or tantalum type capacitors.

Ref. AN1 STABILITY, AN19

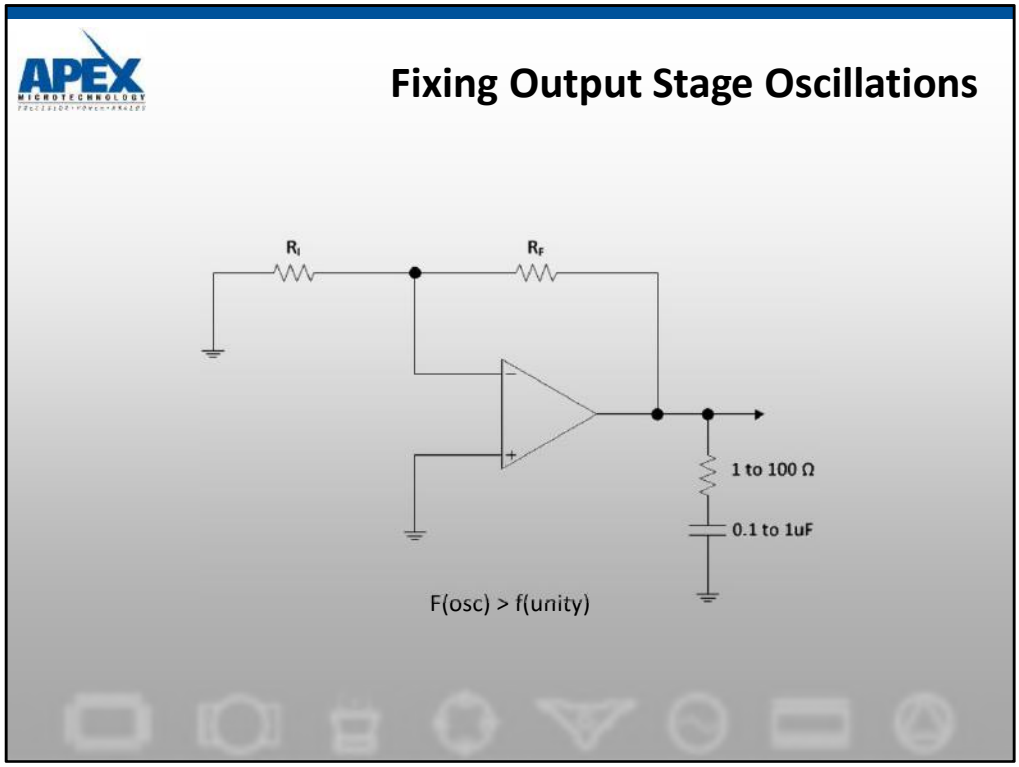


The full complementary output stage is a very easy to use stage. It exhibits symmetric output impedance and low crossover distortion. It is also easy to bias and is inherently stable under most load conditions. Q1 acts as a class A, high voltage gain, common emitter amplifier. Its collector voltage drives the output darlingtons. The bias circuitry provides class AB operation for the output darlingtons, minimizing crossover distortion. Both Q2 and Q3 are only called upon to provide impedance buffering. This is a unity voltage gain, high current gain stage. Both devices are operated as followers and thus provide very low output impedance for either sinking or sourcing current. Monolithic designers are constrained to work with NPN's for handling high currents. For this reason, the "all-NPN" output stage, followed by the "quasi-complementary" output stage were developed.

The quasi-complementary is similar to the full complementary in that Q1 again acts as a class A, common emitter, high gain amplifier and the output devices provide impedance buffering only. Q2 provides the same function as Q2 in a full complementary approach. Q3 and Q4 form a "composite PNP". The inherent problem with this approach is that there is heavy local feedback in the Q3, Q4 loop and this can lead to oscillations driving inductive loads.

The "all-NPN" output stage was an early approach to delivering power in a monolithic. During current source this stage operates much the same as the previous two. The major difference comes about during current sink. During the current sink cycle Q1 changes from a common emitter to an emitter follower. It now provides base voltage drive for Q3. Q3 is operated as a common emitter amplifier. The major disadvantage to this approach is the large changes in both output impedance and open loop gain between source and sink cycles. A problem common to both the quasi-complementary and the all NPN stage is the difficulty of biasing properly over extended temperature range.

Ref. AN1 STABILITY, AN19

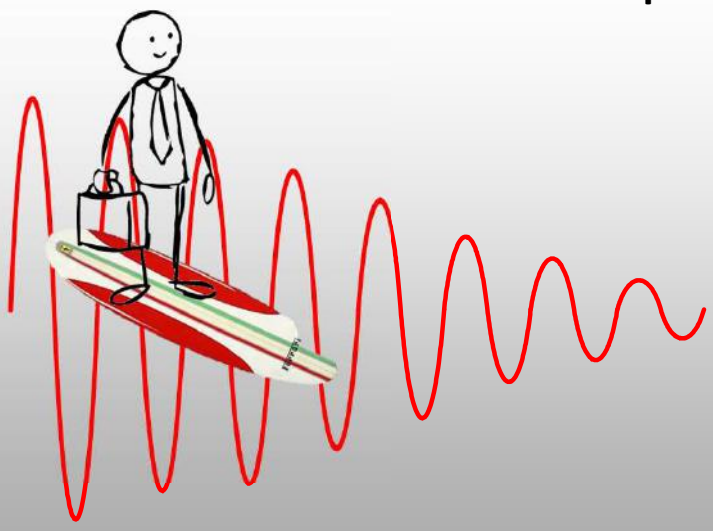


Any time you encounter an oscillation above the unity gain bandwidth of the amplifier it is bound to be one of the output stage problems discussed previously. These can be fixed through the use of a simple “snubber” network from the output pin to ground. This network is comprised of a resistance of from 1 to 100 ohms in series with a .1 to 1 uF capacitor. This network passes high frequencies to ground, thus preventing it from being fed back to the input.

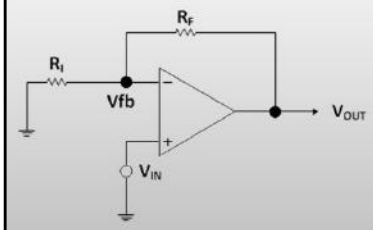
Some manufacturers who use all NPN output stages in their monolithic power amplifiers suggest the use of this type of network to reduce output stage oscillations. Other manufacturers, while having a similar problem, never suggest that this type of network is necessary for proper use. Apex either takes care of the problem internally or specifies specific values for the external network.

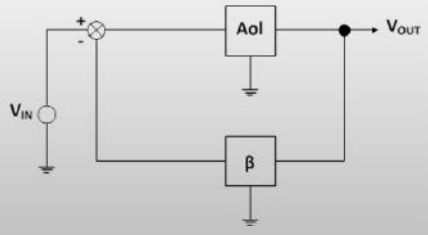
Ref. AN1 STABILITY, AN19

Loop Stability



Beta (β) – Feedback Factor





$\beta = \frac{Ri}{Ri+}$

Vfb = β Vout

$\frac{Vout}{Vin} = \frac{Aol}{1+Aol\beta} = \frac{1}{\beta}$

(For Aol β >> 1)

Vfb = $\frac{Vout*Ri}{Ri+Rf}$ Vout = Vin Aol – Aol β Vout

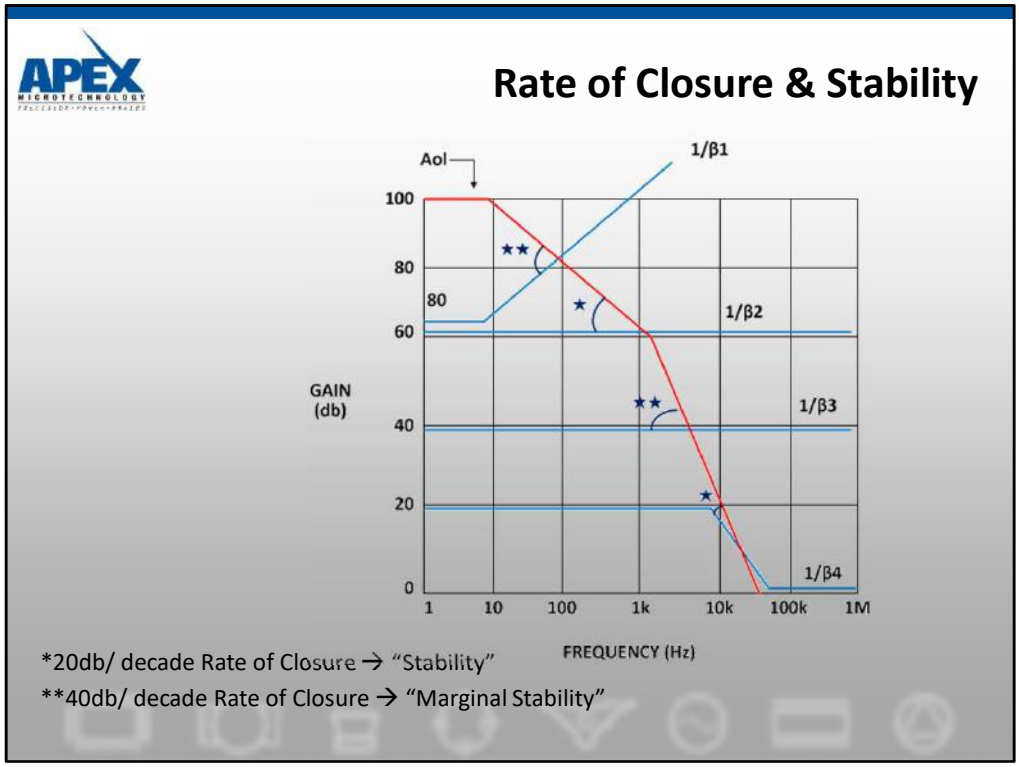
Vfb = β Vout Aol = $\frac{Vout*Aol\beta}{Vout*Vin}$

$\beta = \frac{Ri}{Ri+Rf}$ $\frac{Vout}{Vin} = \frac{Aol}{1+Aol\beta} = \frac{1}{\beta}$

Control theory is applicable to closing the loop around a power op amp. The block diagram above in the right consists of a circle with an X, which represents a voltage differencing circuit. The rectangle with Aol represents the amplifier open loop gain. The rectangle with the β represents the feedback network. The value of β is defined to be the fraction of the output voltage that is fed back to the input. Therefore, β can range from 0 (no feedback) to 1 (100% feedback).

The term Aolβ that appears in the Vout/Vin equation above has been called loop gain because this can be thought of as a signal propagating around the loop that consists of the Aol and β networks. If Aolβ is large there is lots of feedback. If Aolβ is small there is not much feedback (for a detailed discussion of this and other useful topics related to op amps refer to: Intuitive IC Op Amps, Thomas M. Frederiksen, National's Semiconductor Technology Series, R.R. Donnelley & Sons).

Ref. AN19

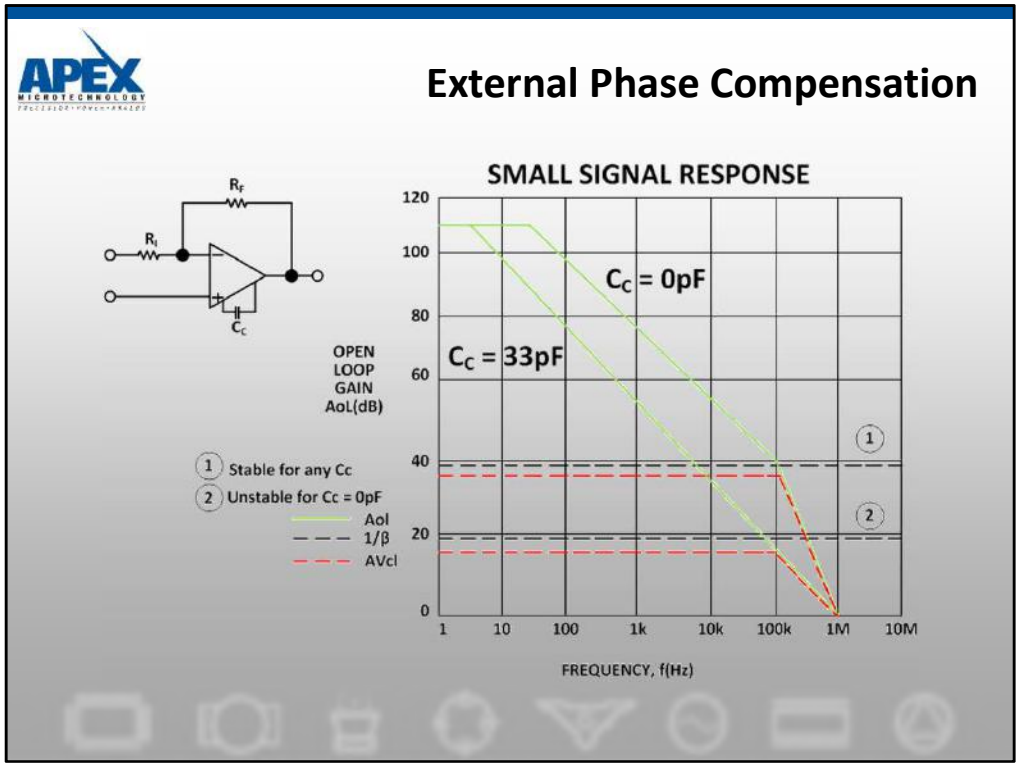


Aol is the amplifier's open loop gain curve. 1/β is the closed loop AC small signal gain in which the amplifier is operating. The difference between the Aol curve and the 1/β curve is the loop gain. Loop gain is the amount of signal available to be used as feedback to reduce errors and non-linearities.

A first order check for stability is to ensure that when loop gain goes to zero, that is where the 1/β curve intersects the Aol curve, open loop phase shift must be less than 180 at the intersection of the 1/β curve and the Aol curve the difference in the slopes of the two curves, or RATE OF CLOSURE is less than or equal to 20 dB per decade. This is a powerful first check for stability. It is, however, not a complete check. For a complete check we will need to check the open loop phase shift of the amplifier throughout its loop gain bandwidth.

A 40 dB per decade RATE-OF-CLOSURE indicates marginal stability with a high probability of destructive oscillations in your circuit. Above examples indicate several different cases for both stable (20 dB per decade) and marginally stable (40 dB per decade) rates of closure.

Ref. AN19, AN38

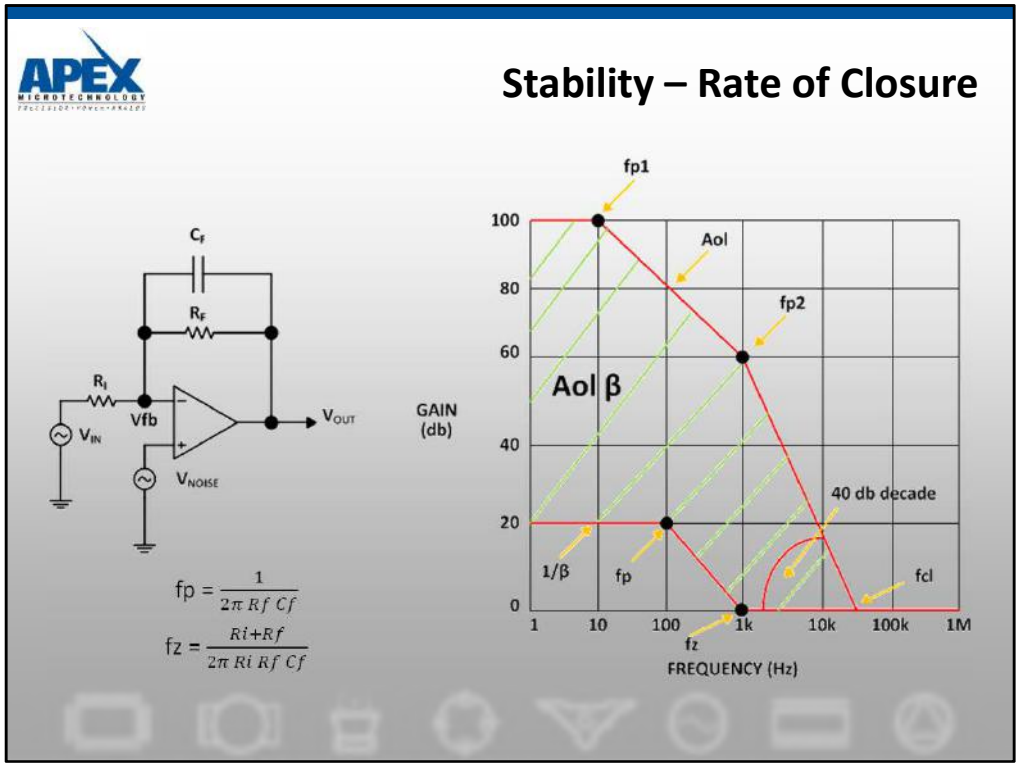


External phase compensation is often available on an op amp as a method of tailoring the op amp's performance for a given application. The lower the value of compensation capacitor used the higher the slew rate of the amplifier. This is due to fixed current sources inside the front end stages of the op amp. Since current is fixed, we see from the relationship of I=CdV/dt that a lower value of capacitance will yield a faster voltage slew rate.

However, the advantage of a faster slew rate has to be weighed against AC small signal stability. In the figure above we see the Aol curve for an op amp with external phase compensation. If we use no compensation capacitor, the Aol curve changes from a single pole response with Cc=33pF to a two pole response with Cc=0pF. Curve 1 illustrates that for 1/β of 40 dB the op amp is stable for any value of external compensation capacitor (20 dB/decade rate of closure for either Aol curve, Cc=33pF or Cc = 0pF).

Curve 2 illustrates that for 1/β of 20 dB and Cc=0pF, there is a 40 dB/decade rate of closure or marginal stability. To have stability with Cc=0pF minimum gain must be set at 40dB. This requires a designer to not only look at slew rate advantages of decompensating the op amp, but also at the gain necessary for stability and the resultant small signal bandwidth.

Ref. AN19, AN38



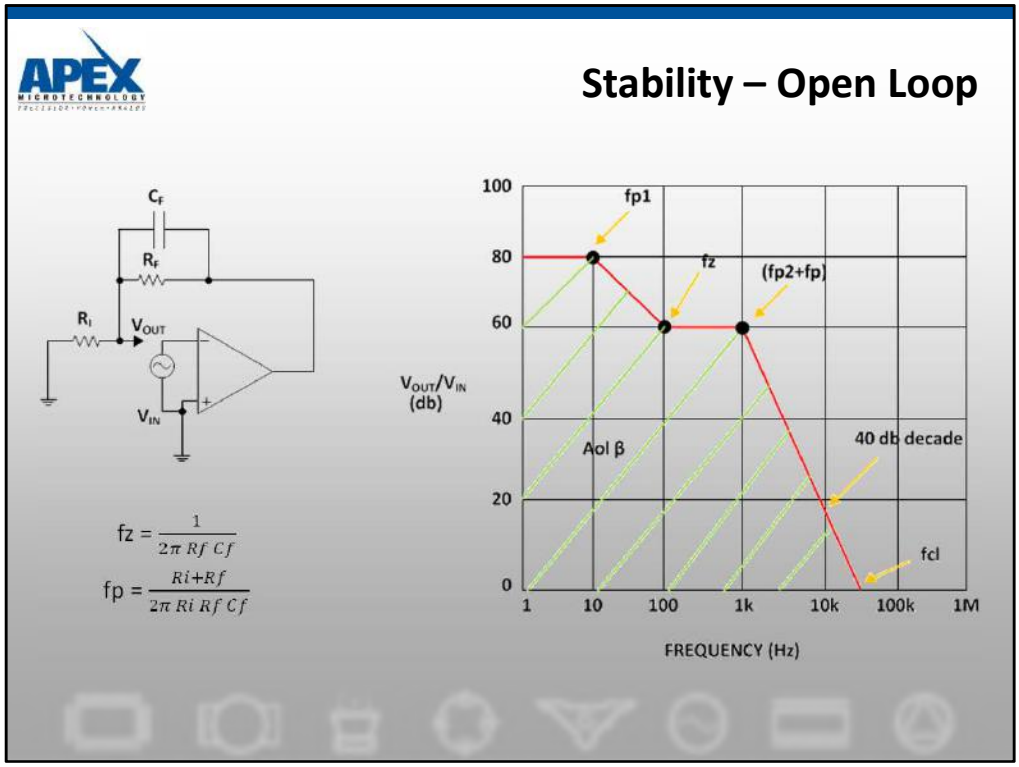
The example above shows a typical single pole op amp configuration in the inverting gain configuration. Notice the additional Vnoise voltage source shown at the + input of the op amp. This is shown to aid in conceptually viewing the 1/β plot.

An inverting amplifier, with its + input grounded, will always have potential for a noise source to be present on the + input. Therefore, when one computes the 1/β plot, the amplifier will appear to run in a gain of 1 + Rf/Ri for small signal AC. The Vout/Vin relationship will still be -Rf/Ri.

The plot above shows the open loop poles from the amplifier's Aol curve as well as the poles and zeroes from the 1/β curve. The locations of fp and fz are important to note as when we look at the open loop stability check we will see that poles in the 1/β plot will become zeroes and zeroes in the 1/β plot will become poles in the open loop stability check.

Notice that at fcl the RATE-OF-CLOSURE is 40 dB per decade indicating a marginal stability condition. The difference between the Aol curve and 1/β curve is labelled Aolβ which is also known as loop gain.

Ref. AN19, AN38



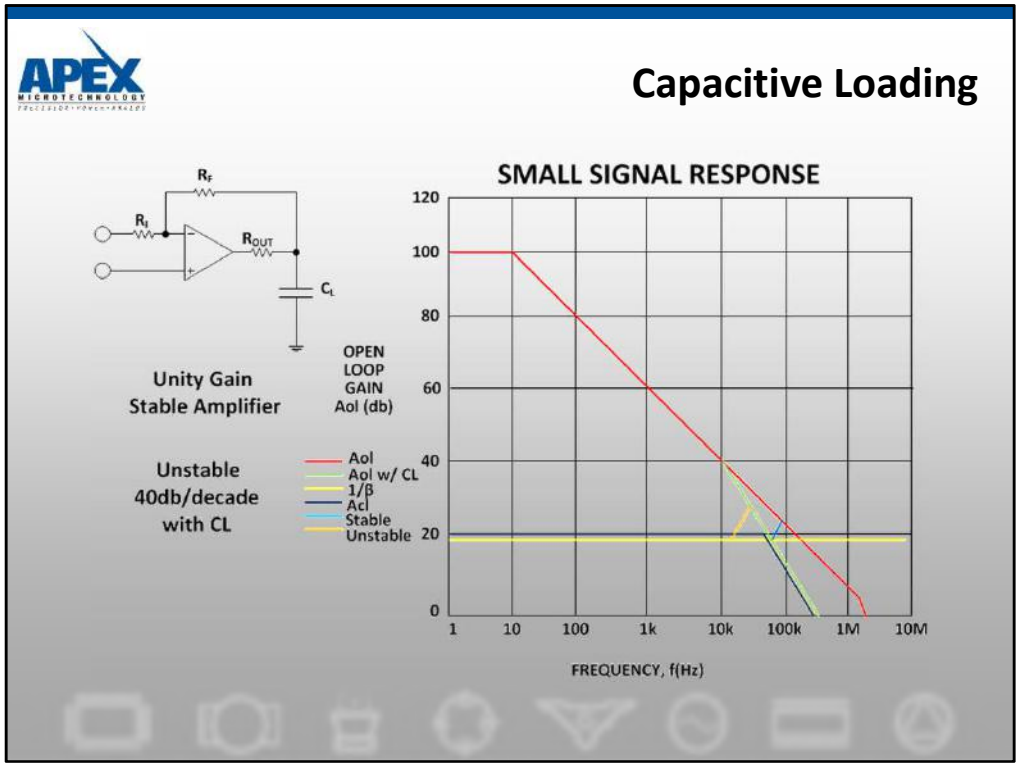
Stability checks are easily performed by breaking the feedback path around the amplifier and plotting the open loop magnitude and phase response. This open loop stability check has the first order criteria that the slope of the magnitude plot as it crosses 0 dB must be 20 dB per decade for guaranteed stability.

The 20 dB per decade is to ensure that the open loop phase does not dip to -180 degrees before the amplifier circuit runs out of loop gain. If the phase did reach -180 the output voltage would now be fed back in phase with the input voltage (-180 degrees phase shift from negative feedback plus -180 degrees phase shift from feedback network components would yield -360 degrees phase shift). This condition would continue to feed upon itself causing the amplifier circuit to break into uncontrollable oscillations.

Notice that this open loop plot is a plot of Aol β. The slope of the open loop curve at fcl is 40 dB per decade indicating a marginally stable circuit. As shown, the zero from the 1/β plot became a pole in the open loop plot and the pole from the 1/β plot became a zero. We will use this knowledge to plot the open loop phase plot to check for stability. This plotting of the open loop phase will provide a complete stability check for the amplifier circuit. All the information we need will be available from the 1/β curve and the Aol curve.

Ref. AN19, AN38

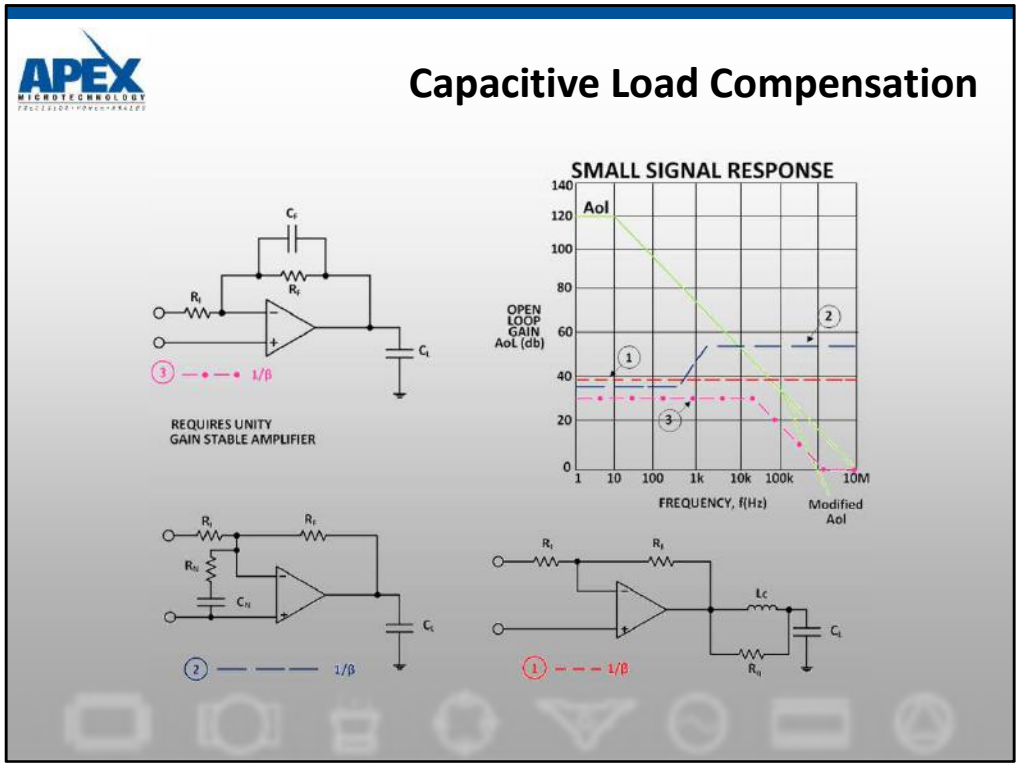
Capacitive Loading



Even when using a unity gain stable amplifier, capacitive loads react with amplifier output impedance, which has the effect of introducing a second pole into the amplifier response which occurs below the unity gain crossover frequency.

If the amplifier is used at a low enough loop gain, this will result in the unstable condition shown in this graph. One simple solution is to increase the close loop again

Ref. AN19, AN25, AN38



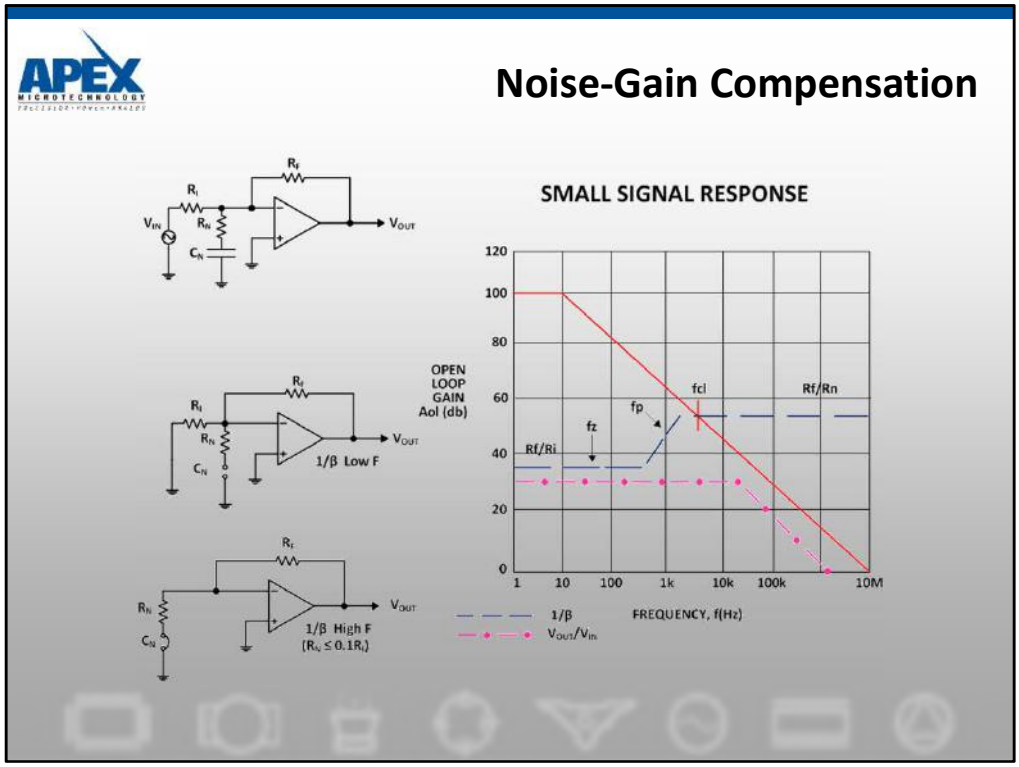
If it's necessary to use low gains with capacitive loads, or in the unlikely event they are a problem at higher gain, these techniques can help solve stability problems caused by capacitive loads.

Method 1 uses a parallel inductor-resistor combination in series with amplifier output to isolate or cancel the capacitive load. Feedback should be taken directly from the amplifier's Aol output. In the graph, this has the effect of restoring the amplifier response to 20db/decade. This method has the advantage that with proper component selection, it can produce an overdamped or critically damped response to a square wave. The inductor is typically 3 to 10µH, and the resistor from 1 to 10 ohms; although a higher voltage, lower current amplifier like PB58 needs about 35µH and 20Ω.

Method 2 uses "noise gain compensation" to enhance stability. This method will work in virtually all cases. The idea is to set the ratio of RF/Rn for a gain high enough to insure crossing the Aol line at a stable point. The capacitor, Cn, is selected for a corner frequency one-tenth the Aol crossover.

Method 3 uses a capacitor in the feedback path to cause a phase lead in the feedback which cancels the phase lag due to capacitive loading. This technique requires careful selection of capacitor value to ensure 1/β crosses the modified Aol before unity gain, unless a unity gain stable amplifier which has a good phase margin is used.

Ref. AN19, AN25, AN38



This plot illustrates how Noise Gain Compensation works. One way to view noise gain circuits is to treat the amplifier as a summing amplifier. There are two input signals into this inverting summing amplifier. One is Vin and the other is a noise source summed in via ground through the series combination of Rn and Cn. Since this is a summing amplifier, Vo/Vin will be unaffected if we sum zero into the Rn-Cn network. However, in the small signal AC domain, we will be changing the 1/β plot of the feedback as when Cn becomes a short and if Rn<<RI the gain will be set by RF/Rn. The figure above shows the equivalent circuits for AC small signal analysis at low and high frequencies.

Notice in the plot above that the Vo/Vin relationship is flat until the Noise Gain forces the loop gain to zero. At that point, fcl, the Vo/Vin curve follows the Aol curve since loop gain is gone to zero. Since noise gain introduces a pole and a zero in the 1/β plot, here are a few tips to keep phase under control for guaranteed stability. Keep the high frequency, flat part of the noise gain no higher in magnitude than 20dB greater than the low frequency gain. This will force fp and fz in the above plot to be no more than a decade apart. This will also keep the open loop phase from dipping below –135 since there is usually an additional low frequency pole due to the amplifier's Aol already contributing an additional –90 degrees in the open loop phase plot. Keep fp one-half to one decade below fcl to prevent a rate of closure of 40dB per decade and prevent instability if the Aol curve shifts to the left which can happen in the real world. Usually one selects the high frequency gain and sets fp. fz can be gotten graphically from the 1/β plot. For completeness here are the formulae for noisegain poles and zeroes:

fp = $\frac{1}{2\pi RnCn}$ fz = $\frac{RF+R}{2\pi\,(Cn)(RFRI+RFRn+R\quad)}$ Ref. AN19, AN25, AN38

PowerDesign Cload

STABILITY FOR CAPACITIVE LOADS — 45 Goto Composite

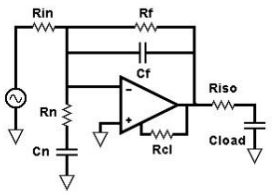
MODEL	PA07	Note/PBs	Rn	99999999	Kohms	Estimated Closure Frequency =	36.51741	KHz
Rcl	0.4	Ohms	Cn	0	nF	Suggested maximum bandwidth	8.659643	KHz
Cload	4	uF	Cf	0	pF	Estimated Closure Rate =	40.0	db/decade
Rin	2	Kohms	Riso	0	Ohms	Estimated Phase Margin =	25.8688	Degrees
Rf	20	Kohms						
Notes:								

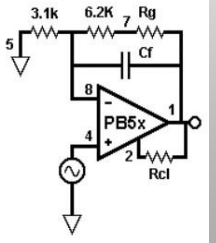
R-C Pole Calculator:

20	Kohms	0.1	Kohms	30	KHz	28 Print Data, Bode & Phase	29 Print Data, Bode, Phase & Parts
20	KHz	10	nF	4	uF		
0.3979	nF	159.15494	KHz	1.326291192	Ohms		

Total Rout	2.9	Ohms
Pole Zout/Cload	13.720253	KHz
1/Beta (DC)	20.8	db
Noise Gain	0.0	db
Pole Noise Gain	15.915494	KHz
Zero Noise Gain	15.915487	KHz
Pole Cf/Rf	7.958E+09	KHz
Zero Rf/Cf	8.754E+10	KHz
Zero Riso/Cload	3.979E+09	KHz

Page Down for Plots.



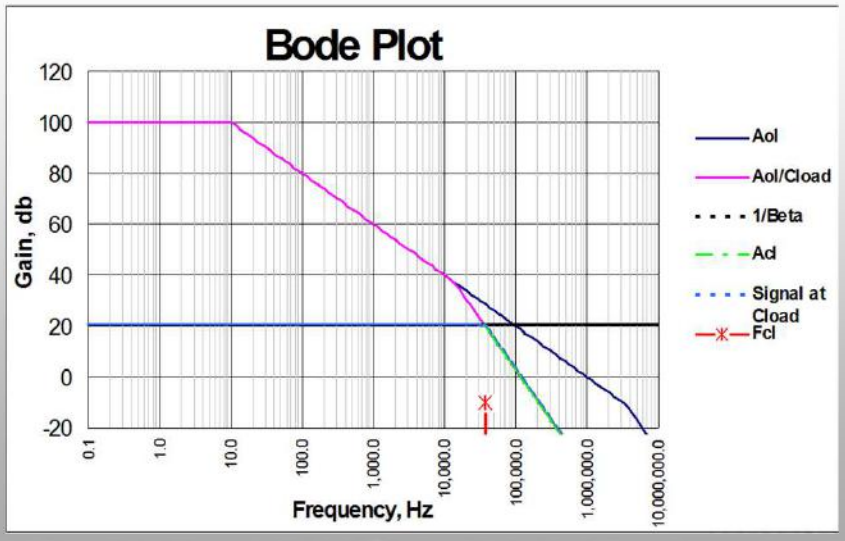


This basic circuit will demonstrate how each of the capacitive load compensation techniques can work independently to solve the large C load stability problem.

This screen sets up the problem. Enter values describing the circuit being sure to assign open values to components not yet in the circuit. To the right we see a 40db closure rate and less than 30°phase margin. We don't need them yet but please note the three windows of the R-C Pole Calculator . The first window tells us 398pF will yield a pole at 20KHz when paralleled with 20K. The last window tells us 1.3Ω will place the corner frequency at 30KHz when in series with 4µF.

Ref. AN38

PA07/Cload Problem



This picture is the first part of the problem. The output impedance of the PA07, plus the current limit resistor along with the big capacitive load, have added an additional pole to the open loop response of the amplifier. This degrades closure rate to 40db per decade--a warning flag. Its too bad we can't use a gain of 100 (40db) where closure rate would have been OK.

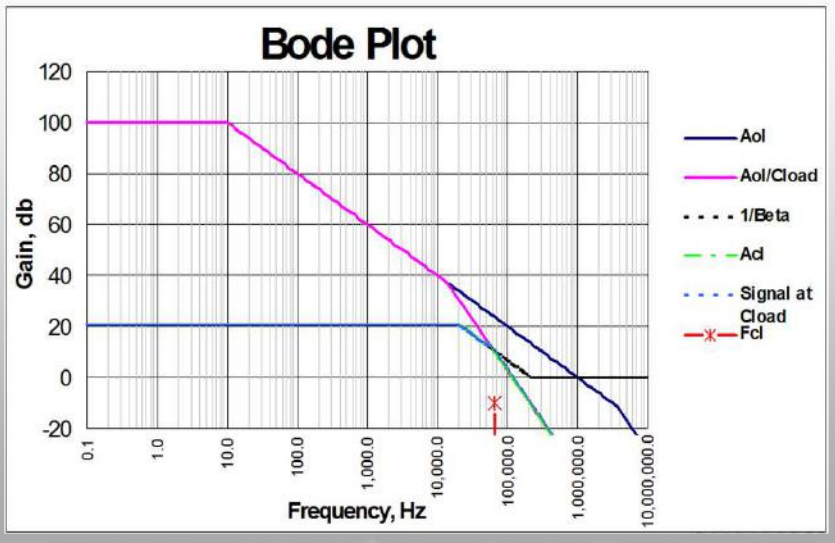
Here's the beauty of this system: Visualize or hold anything with a straight edge up to the graph in the area where we just learned a roll-off capacitor fixes these problems. Hold the edge parallel to the original open loop response curve and move it around to achieve intersection with the modified response about ½ way between 0 & 20db. Read the frequency where the straight edge crosses 20db. Remember the 20KHz in the R-C Pole Calculator? This is the origin. The spreadsheet makes it very easy to play "what if".

For noise gain compensation, visualize the upper flat portion of the curve being 20db up from the DC gain. Setting Rn = Rin/9 will put you about where it should be. On the open loop gain curve, read frequency where the imaginary line crosses. Enter one tenth this frequency and the Rn value in the R-C Pole calculator to set Cn. Again, play what if to optimize the circuit.

For Riso pick a frequency a little lower than the intersection of DC gain and the modified open loop gain. It looks like 30KHz is about as high as we should go. Use the R-C Pole Calculator, plug in values and optimize.

Ref. AN38

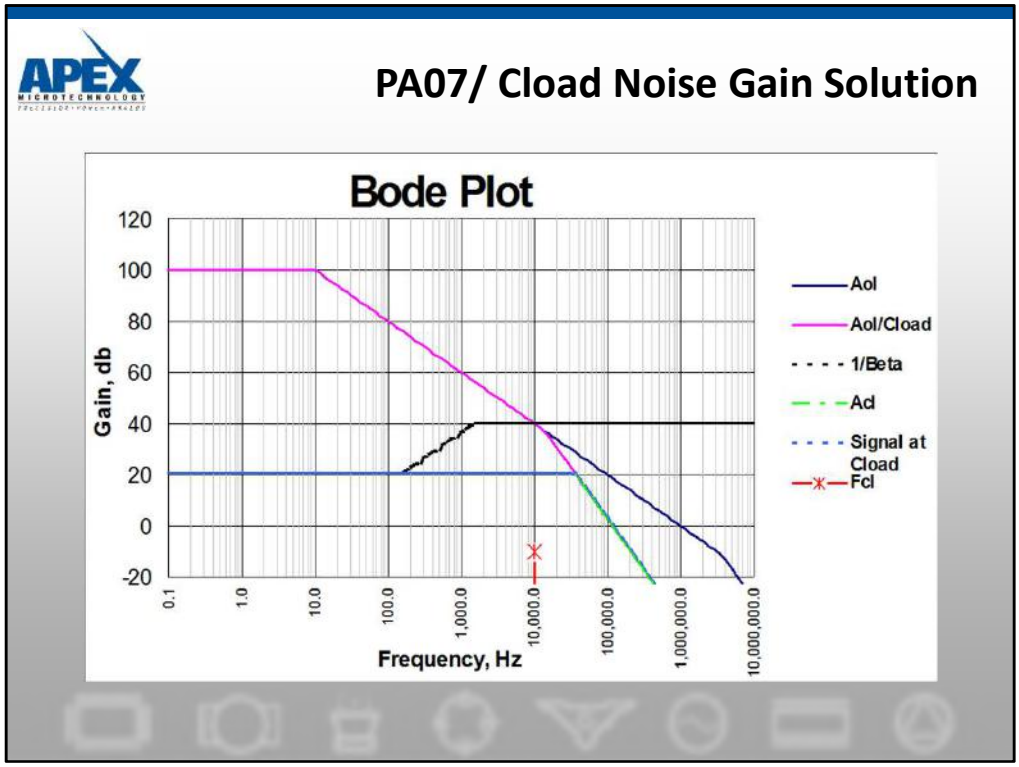
PA07/Cload Cf Solution



A 390pf capacitor yields 61 ° phase margin.

Time to use or vision again to discover a very important trap NOT to fall into.
The trap: If a little capacitor is good, a bigger one should be better.
The problem: 1/β never goes below 0db.

Visualize a line segment for 3.9nF capacitor starting down at 2KHz, then turning horizontal at 0db. Intersection rate is again 40db/decade and phase margin will drop to 16°!

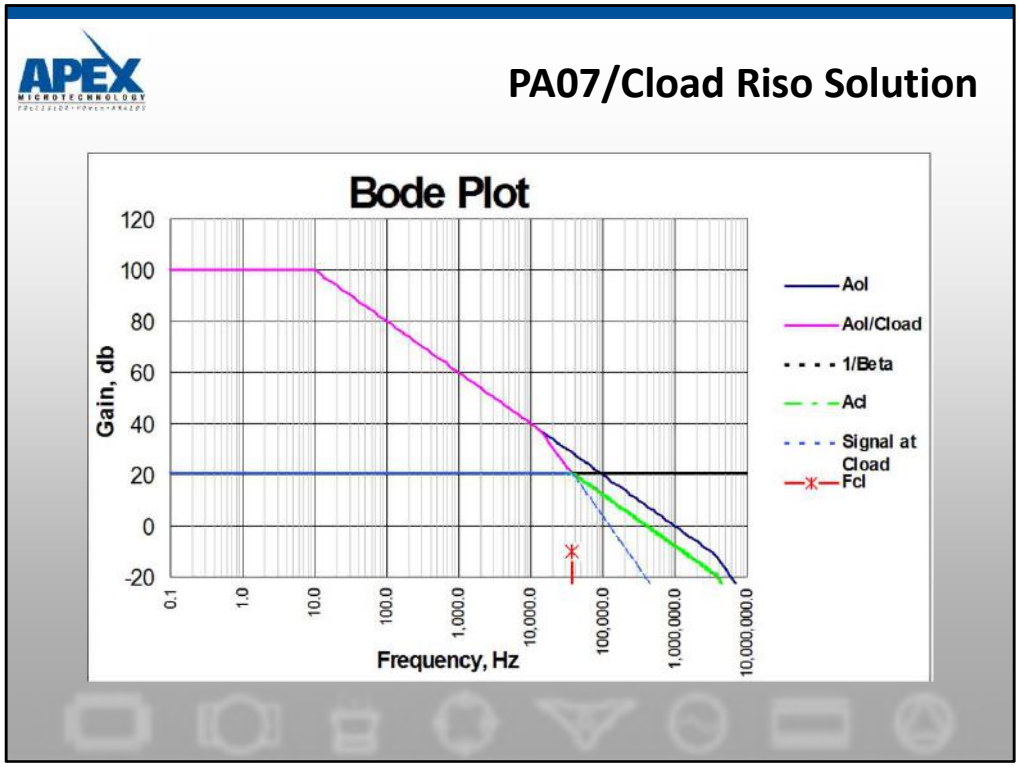


An important point one more time:

The closed loop curves here 1/β curves

They are obviously related to signal gains but are stability analysis tools which always assume non-inverting gain. A signal gain of -1 will plot as 2 in 1/β format. The signal gain does not increase between 150Hz and 1.5KHz.

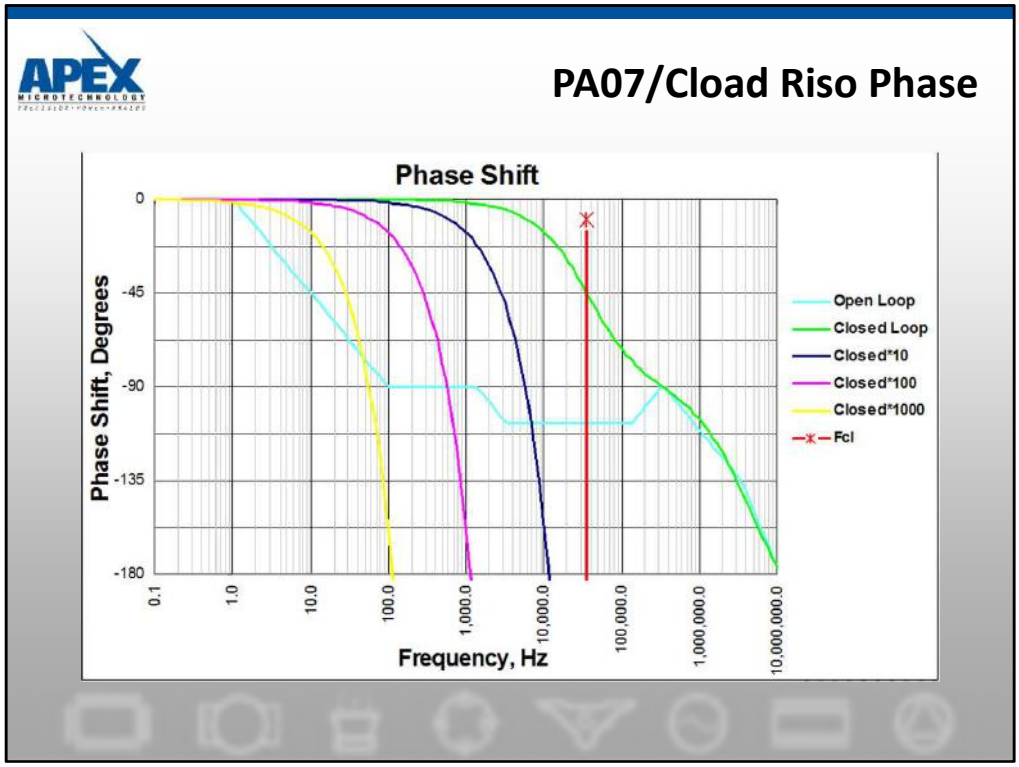
Ref. AN38



Notice the difference between the curve showing the Signal at Cload and the Acl curve. This is the voltage loss across Riso which is outside the feedback loop and therefore not corrected for amplitude loss. The picture says we really aren't loosing much at usable frequencies. Lets look at another error between 10KHz and closure frequency.

Op amp theory says output impedance is reduced by the loop gain. Our data entry screen told us Zout for the PA07 was 5Ω. This graph tells us loop gain goes from 10 to zero in our band of interest. This means uncorrected output impedance goes from 0.5 to 5Ω in this band. The losses across the 1.2Ω Riso now seem even more trivial.

Ref. AN38

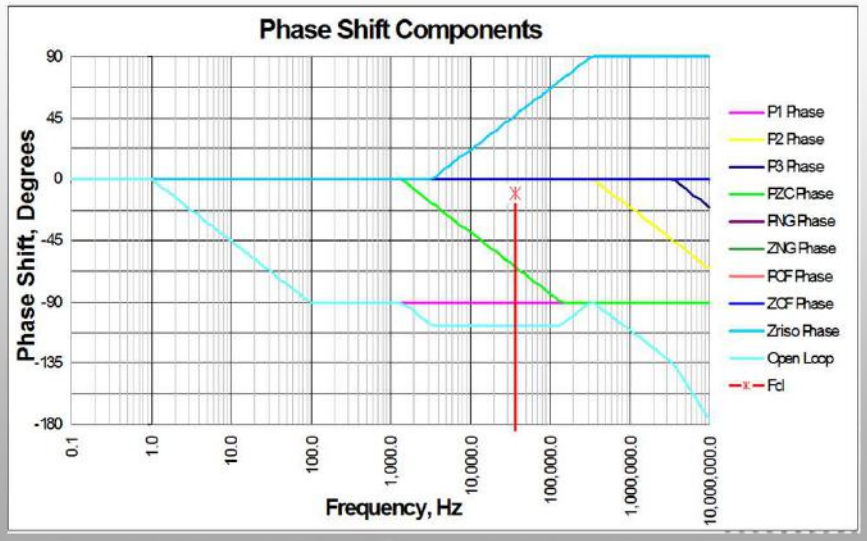


The first thing usually pulled from this graph is phase margin; 45°is good, 30°is pushing things. Here we see the open loop phase crossing Fcl (closure frequency) at 107¼°(Excel97 gives you the number if you place the cursor on the curve). Phase margin = 180°- open loop phase shift, or 72.75°in this case.

Sometimes we need to know the closed loop phase shift at a particular frequency. Suppose 1KHz is the point of interest. We can tell from the un-scaled curve this shift is not zero but resolution stinks. The curve with best resolution at 1KHz is the one scaled times 100. This curve crosses 1KHz at 158.66°for an open loop phase of about 1.6°.

Ref. AN38

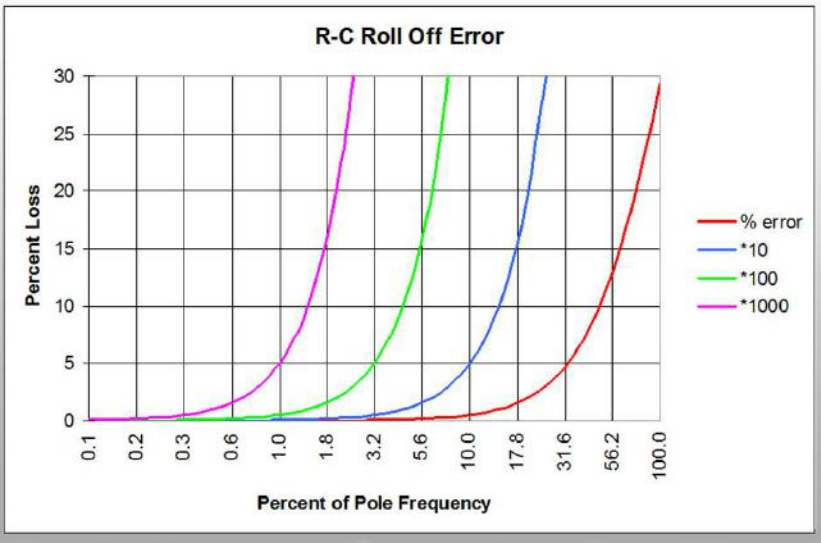
PA07/Cload Riso Phase Components



Here are all the pieces making up the total open loop phase shift. Each segment is based on component values and the plotting rules detailed in Application Notes 19 and 25. P1 Phase (first pole in the bode plot) appears to be missing. Power Design shows only one curve when two or more coincide. Notice that P1 Phase does show up roughly between 1KHz and 100KHz. Open loop Phase is simply the sum of all the segments. Some segments show only partially or not at all because they are off scale, usually because of the open values entered.

Ref. AN38

Errors of Straight Lines

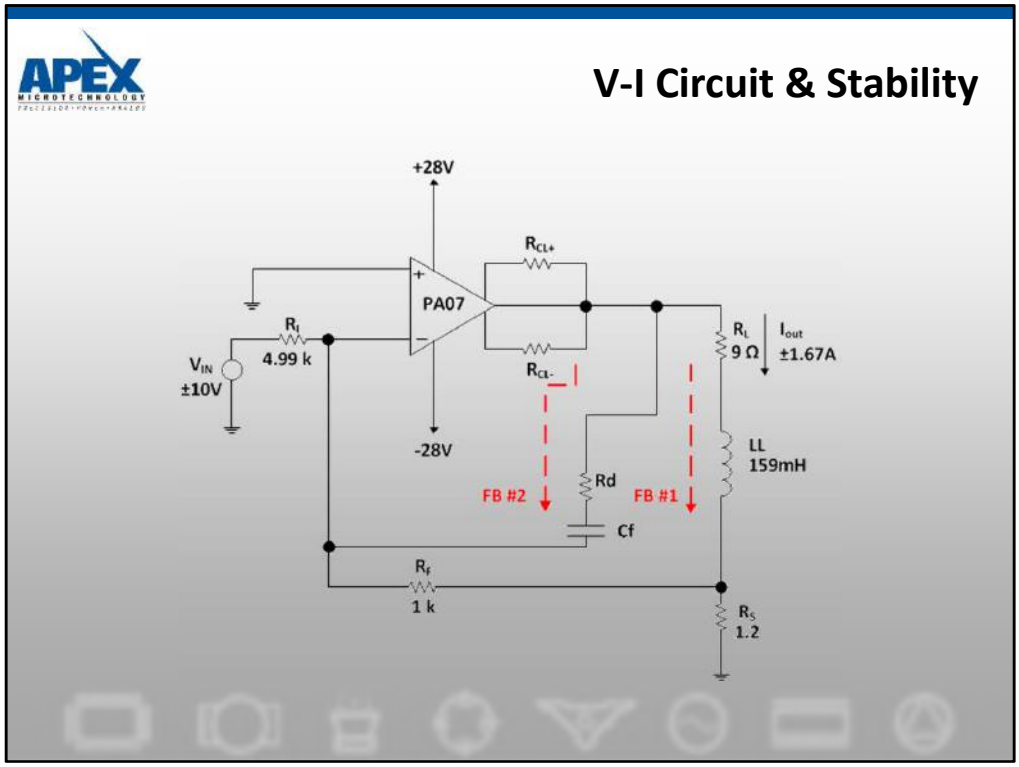


Straight line approximation is a great way to visualize location of corner frequencies but information is lost about attenuation near the corner. In db terms, the errors are small numbers and most circuits have enough frequency margin such that we see no problems.

In more exacting circuits, this graph indicates about 30% low amplitude right at the corner frequency, a 10.6% error at half the corner frequency, 3% at onequarter, and so on.

These errors apply to both the use of an isolation resistor and to a roll-off capacitor in the feedback loop.

Ref. AN38



This V-I (Voltage to Current) topology is a floating load drive. Neither end of the load, series RL and LL, is connected to ground.

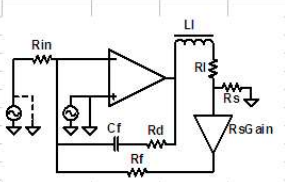
The easiest way to view the voltage feedback for load current control in this circuit is to look at the point of feedback which is the top of Rs. The voltage gain VRs/Vin is simply –RF/RI which translates to (–1K/4.99K = –.2004). The Iout/Vin relationship is then VRs/Rs or Iout = –Vin(RF/RI)/Rs which for this circuit is Iout = –.167Vin .

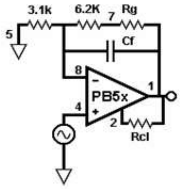
We will use our knowledge of 1/β, Rate of Closure, and open loop stability phase plots, to design this V-I circuit for stable operation. There are two voltage feedback paths around the amplifier, FB#1 and FB#2. We will analyze FB#1 first and then see why FB#2 is necessary for guaranteed stability.

Ref. AN19

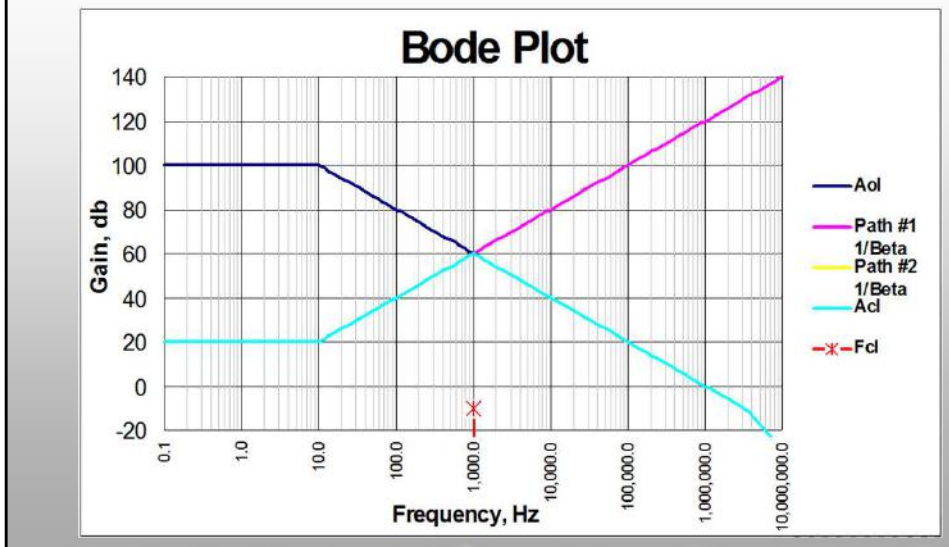
PA07 Inductive Load Problem Entry

	A	B	C	D	E	F	G	H	I	J	K	L
1	**STABILITY FOR INDUCTIVE LOADS**											
2	MODEL	PA07	Note/PBs	Rin	4.99	Kohms	Estimated Closure Frequency =			1	KHz	
3	Rs	1.2	Ohms	Rf	1	Kohms	Suggested maximum bandwidth			562.3413	Hz	
4	Lload	159	mH	Cf	99999	nF	Estimated Closure Rate =			40.0	dB/decade	
5	Rload	9	Ohms	Rd	999999999	Kohms	Estimated Phase Margin =			0.41	Degrees	
6	Rs Gain	1	Is this a Composite?		No							
7	Notes:											
8	**R-C Pole Calculator +**		Value Suggestions:				28 Print Data, Bode & Phase		29 Print Data, Bode, Phase & Parts			
9	45	Kohms	Rd Kohms	82.47245	AC gain dB	22						
10	8	Hz	Rd Kohms	10	Rd Kohms	9.654487						
11	442.1	nF	Cf nF	1.11E-06								
12												
13	Ri/(Ri+Rf)		0.833055092									
14	Equiv Z @ Rs		1.2	Ohms								
15	Requiv/(Rl+Requiv)		0.117647059									
16	DC Beta		0.098006481									
17	DC Gain		20.17490405	dB								
18	Zero R/L		10.20993975	Hz								
19	Rin||Rf		0.833055092	Kohms								
20	Zero Rd/Cf		1.59157E-09	Hz								
21	AC Gain		181.5865255	dB								
22	Zero Cross		1000	Hz								





Aol & FB#1 Magnitude Plot for Stability

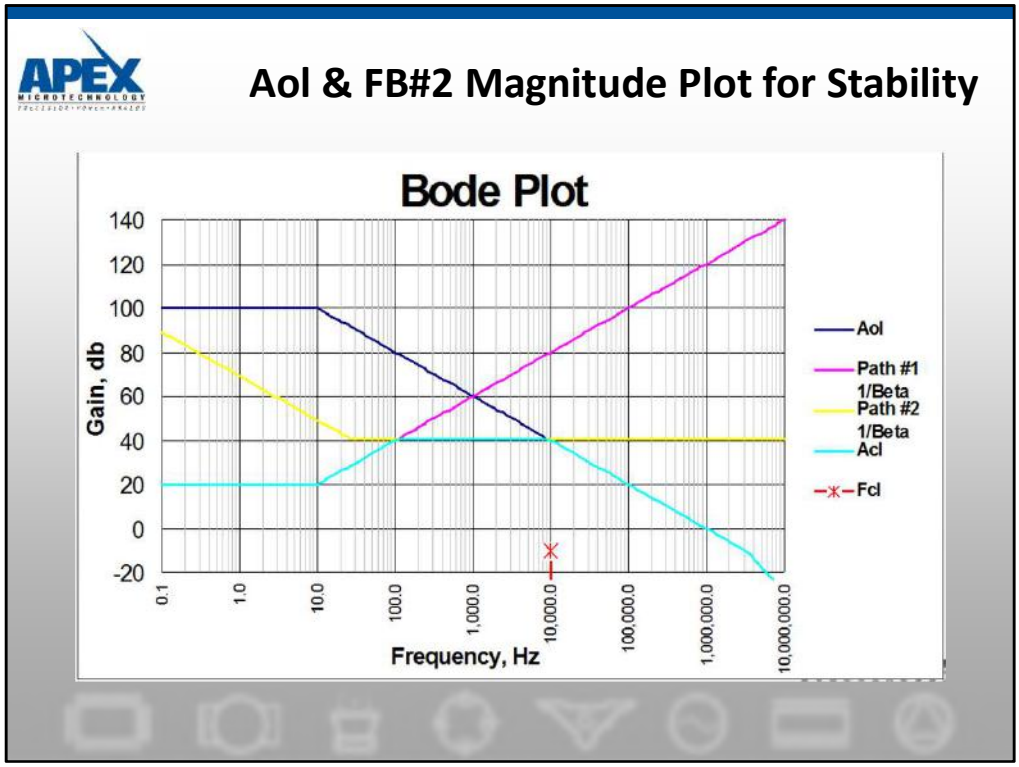


As frequency increases, impedance of the inductor increases and being inside the feedback loop it is causing closed loop gain to increase. Another way to view it: The amplifier's job is to drive constant current but as frequency goes up it needs more voltage to maintain that constant current, so voltage gain is increasing with frequency.

Open loop gain is decreasing 20db per decade and closed loop gain is increasing 20db per decade. This intersection rate of 40db per decade is the problem.

What if we could invent a circuit to make the open loop gain stop increasing? The precise function of feedback path #2! As soon as we enter this in the data entry screen, we see 20db per decade and phase margin of 45°.

Ref. AN19,AN38



Here's a way to start:

1. Select Rd for an AC gain either 20db below gain at the intersection or 20db above the DC gain of the current feedback (Path 1). These two points are the two suggested Rd values on the data entry screen. We can also read 40db from the graph and enter it as AC gain. An 82K should work well.

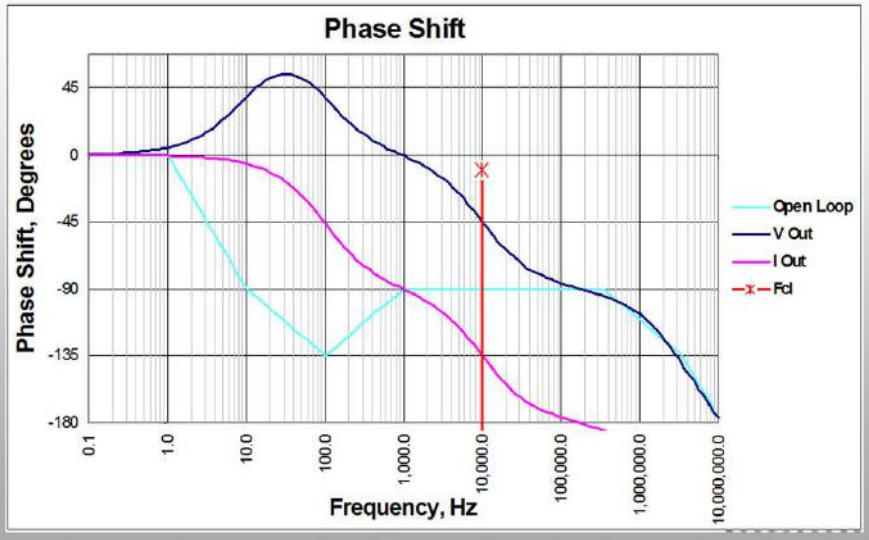
2. Select Cf for a corner frequency ½ to 1 decade below the intersection frequency. Giving the calculator pad 82K and 30Hz allows it to suggest a standard value of 68nF (with a little help from you). After entering 82K for Rd, the data entry screen will suggest a capacitor based on 1 decade below the intersection frequency.

3. Play "what if" with the circuit.

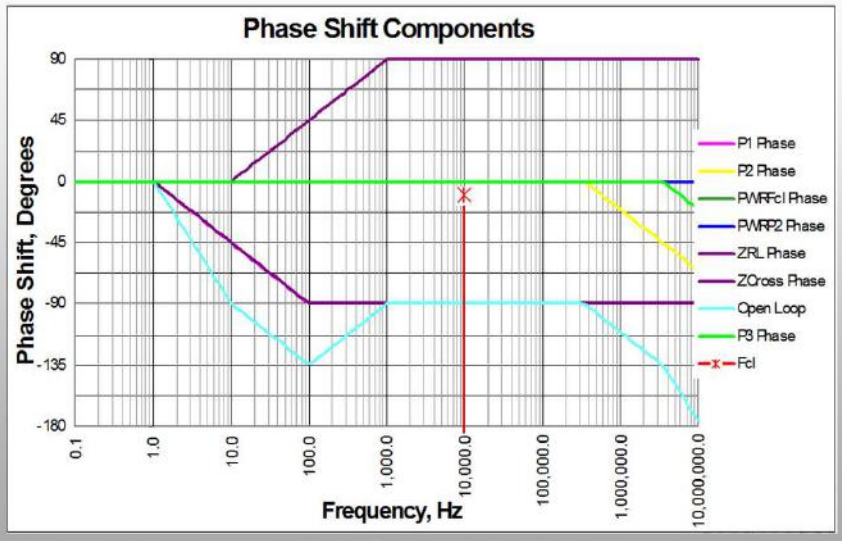
4. If trying to achieve higher bandwidth, try increasing the value of Rs.

Ref. AN19,AN38

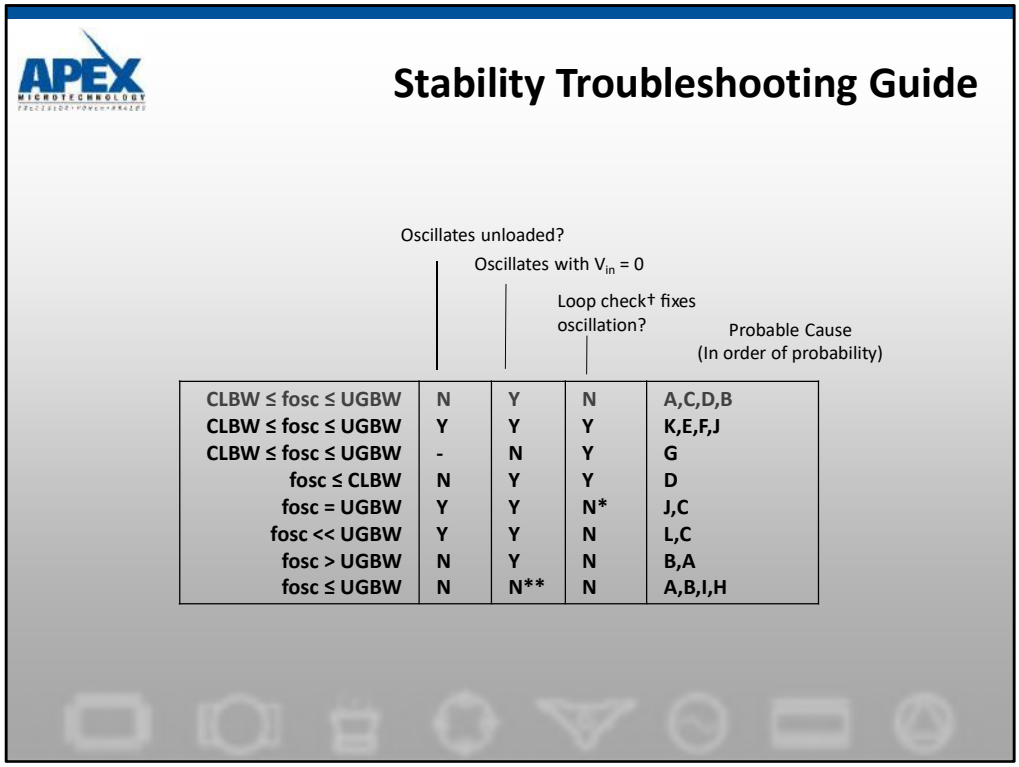
Phase Plot for Stability



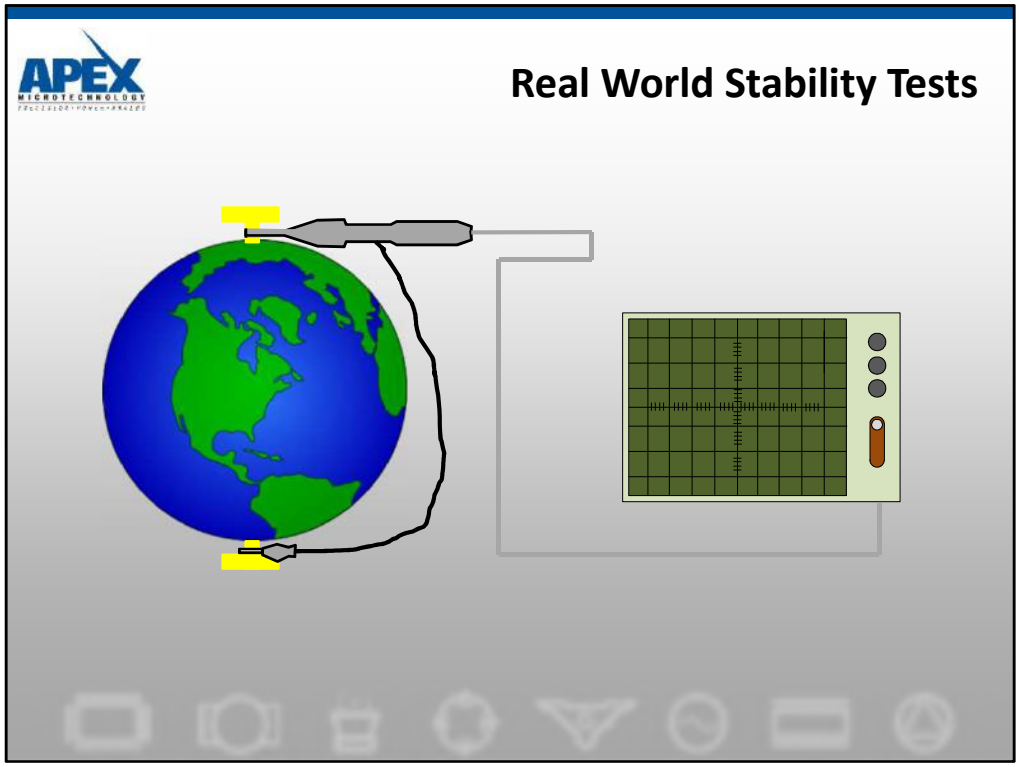
Phase Shift Components



Here are all the pieces going into the previous phase plot. Again, Application Note 19 is the reference.



Previous sections have covered the major stability issues for more details and further explanation to use the Stability Troubleshooting Guide, refer to Application Note 1 “General Operating Considerations”
Ref. AN1 STABILITY



We have devoted much text to discussing and learning how to design stable circuits. Once a circuit is designed and built it is often difficult to open the feedback path in the real world and measure open loop phase margin for stability.

The following Real World Stability Tests offer methods to verify if predicted open loop phase margins actually make it to the real world implementation of the design. Although the curves shown for these tests are only exact for a second order system, they provide a good source of data since most power op amp circuits possess a dominant pair of poles that will be the controlling factor in system response.

When performing these tests, use actual production hardware. Supplies, harnesses, mechanical loads, fluid load and others all make a difference. The time spent here may save days of troubleshooting 6 months after the design is in production.

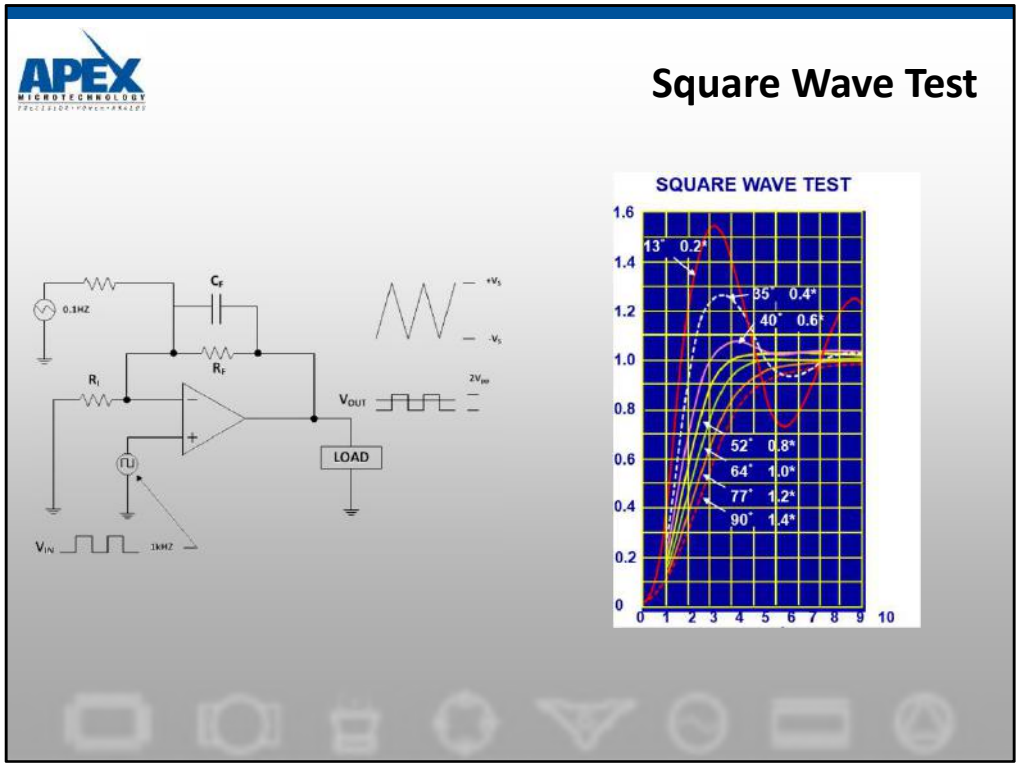


Figure 40 illustrates the Square Wave Test for measuring open loop phase margin by closed loop tests. The output amplitude of the square wave is adjusted to be 2 Vpp at a frequency of 1 kHz. The key elements of this test are to use low amplitude (AC small signal) and a frequency that will allow ease of reading when triggered on an oscilloscope. Amplitude adjustment on the oscilloscope wants to accentuate the top of the square wave to measure easily the overshoot and ringing. The results of the test can be compared to the graph in Figure 40 to yield open loop phase margin.

A complete use of this test is to run the output symmetrical about zero with +/-1V peak and then re-run the test with various DC offsets on the output above and below zero. This will check stability at several operating points to ensure no anomalies show up in field use

Ref. AN19

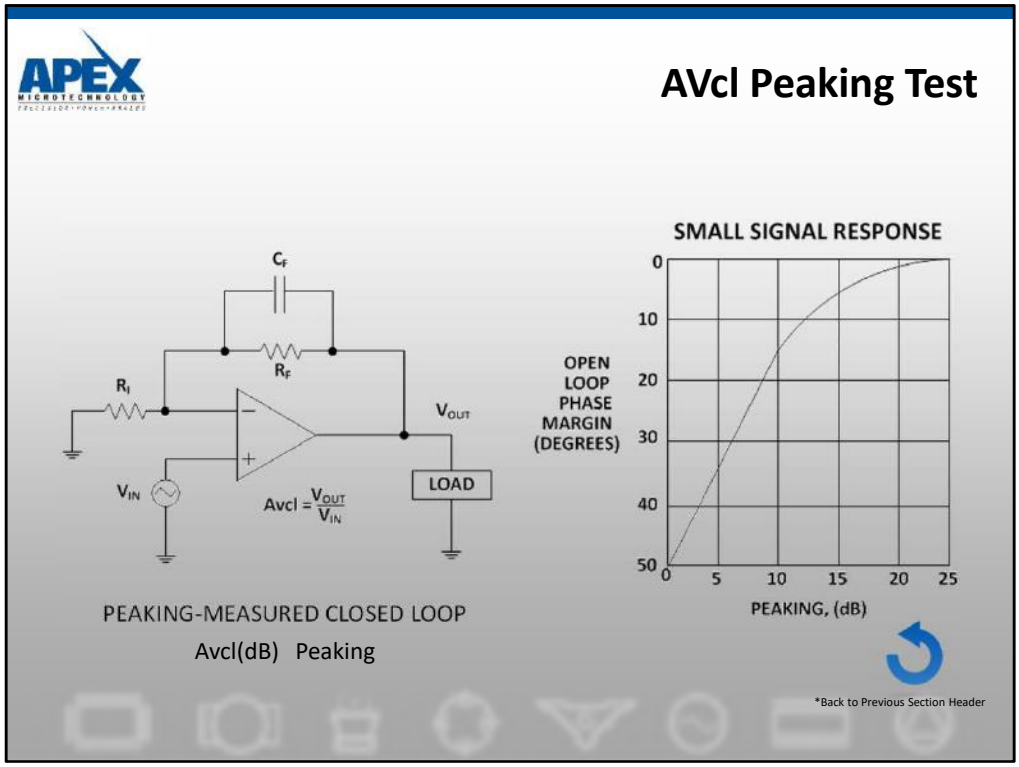


Figure 39 illustrates the AVcl Peaking Test for measuring open loop phase margin in the real world closed loop domain. From the closed loop Bode plot, we can measure the peaking in the region of gain rolloff.
This will directly correlate to open loop phase margin as shown.

We are often asked to generate data resembling this test. Why not look up the graph and translate to degrees of phase margin?

Ref. AN19