SAFE OPERATING AREA (SOA)

Safe Operating Area

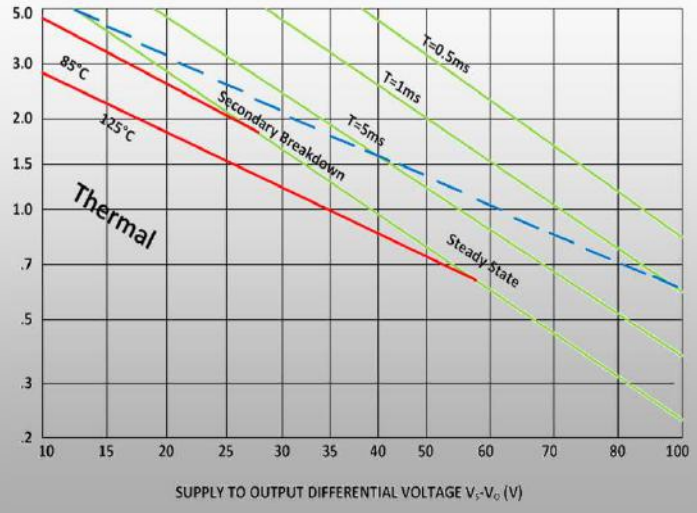
Output Stage Danger!

- Current Handling Limitations
- Thermal (Power) Limitations
  - Steady State
  - Transient/Pulse Operation
- Second Breakdown
  - Bipolar Devices
  - MOSFETs: Not Applicable

Using the SOA Curve

$Ø_{jc}$ = 2.6°C/W

T_j (MAX) = 200°C

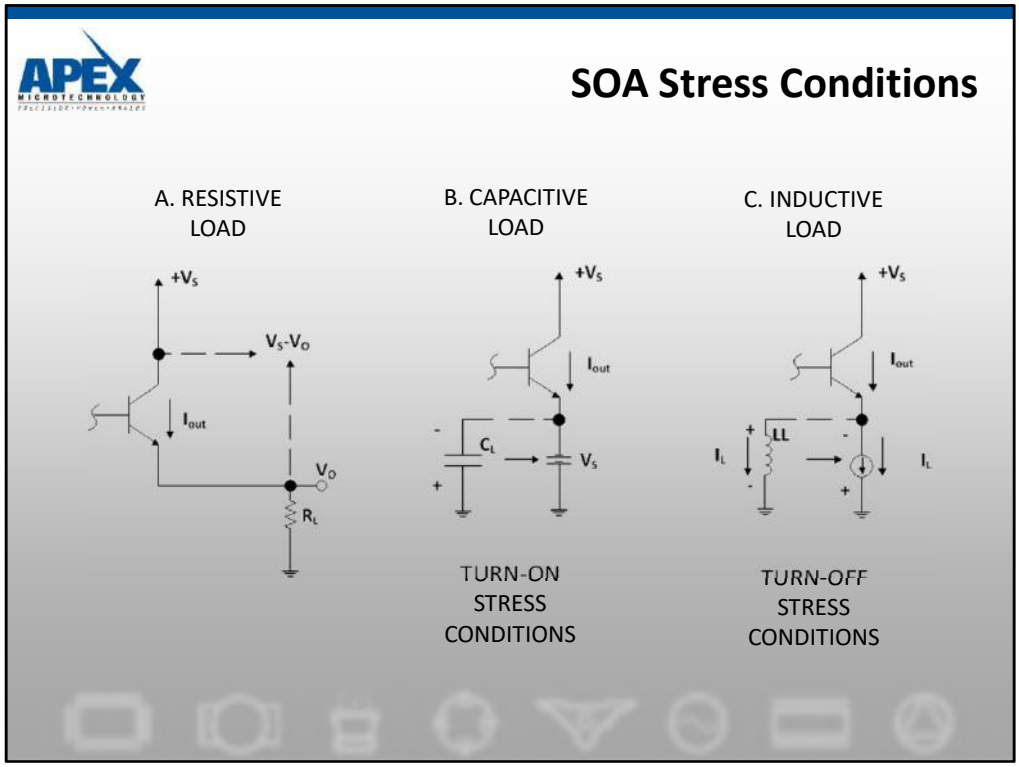


Safe operating area curves show the limitations on the power handling capability of power op amps. There are three basic limitations.

The first limitation is total current handling capability. A horizontal line or the top of the SOA curve and represents the limit imposed by conductor current handling capability die junction area and other current density constraints. The second limitation is total power handling capability or power dissipation capability of the complete amplifier. This includes both of the power die and the package the amplifier is contained in. Note that the product of output current on the vertical axis and Vs-Vo on the horizontal axis is constant over this line. The third portion of the curve is the secondary breakdown areas. This phenomenon is limited to bipolar devices. MOSFET devices do not have this third limitation. Secondary breakdown is a combined voltage and current stress across the device.

Although the constant current boundary and the secondary breakdown boundary remain constant, the constant power/thermal line moves toward the origin as case temperature increases. This new constant power line can be determined from the de-rating curves on the data sheet. The case temperature is primarily a function of the heat sink used.

The dashed line was constructed in this manner for Tc = 25°C for an amplifier advertised as a 67W device (PA07 or PA10). In addition to the fact that very few applications exhibit Tc=25°, secondary breakdown prohibits DC operation over its entire length!



On the SOA graph, the horizontal axis, $V_S–V_O$ does not define a supply voltage or total supply voltage or the output voltage. IT DEFINES THE VOLTAGE STRESS ACROSS THE CONDUCTING DEVICE. Thus $V_S–V_O$ is the difference from the supply to the output across the transistor that is conducting current to the load. The vertical axis is simply the current being delivered to the load.

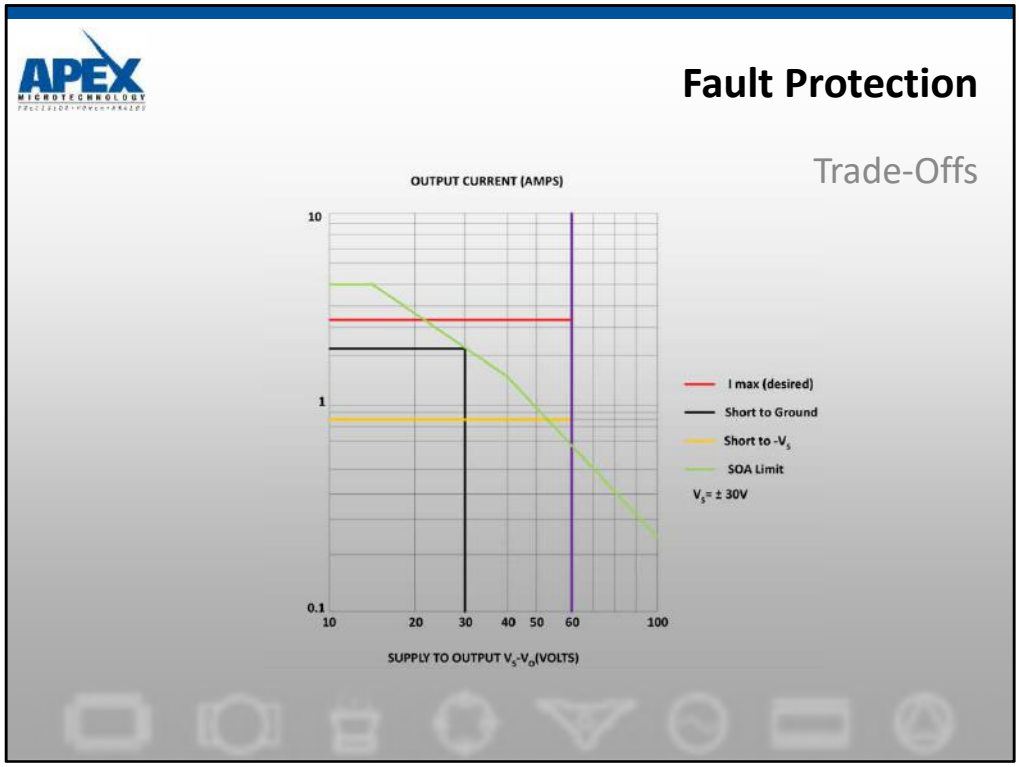
For resistive loads maximum power dissipation in the amplifier occurs when the output is 1/2 the supply voltage. This is because when the output is at 0 volts, no current flows from the amplifier whereas at maximum load current very little voltage is across the conducting transistor since the output voltage is near the supply voltage.

For reactive loads this is not the case. Voltage/current phase differences can result in higher than anticipated powers being dissipated in the amplifier.

An example of an excessive stress condition created by a capacitive load is shown in Figure B. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a “go positive” signal. Immediately the amplifier will deliver its maximum rated output current into the capacitor which can be modeled at t = 0 as a voltage source. This leads to a stress across the conducting device of Imax X total supply voltage($2V_S$).

Figure C shows a similar condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the conductor has built up to some value IL. Now the amplifier is given a “go negative” signal which causes the output voltage to swing to down near the negative supply. However the inductor at time t = 0 can be modeled as a current source still drawing IL. This leads to the same situation as before, that is total supply voltage across a device conducting high current.

Ref. AN1 SAFE OPERATING AREA, AN22



Current limit can be used to protect the amplifier against fault conditions. If, for instance, it is desired to protect the amplifier against a short-to-ground fault condition the Vs-Vo number on the horizontal axis is equal to Vs since Vo is zero. Following this value up to the power dissipation limit and then across to the output current gives the value of current limit necessary to protect the amplifier at that case temperature. Note that better heat sinking allows higher values of current limit.

For more aggressive fault protection it may be desired to protect the amplifier against short to either supply. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the Vs-Vo axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit.

It is often the case that requirements for fault protection and maximum output current may conflict at times. Under these conditions there are only four options. The first is simply to go the an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called “foldover” or “foldback.” This is available on some amplifiers such as the PA10 and PA12.

Ref. AN1 SAFE OPERATING AREA, AN22

Current Limit Definition

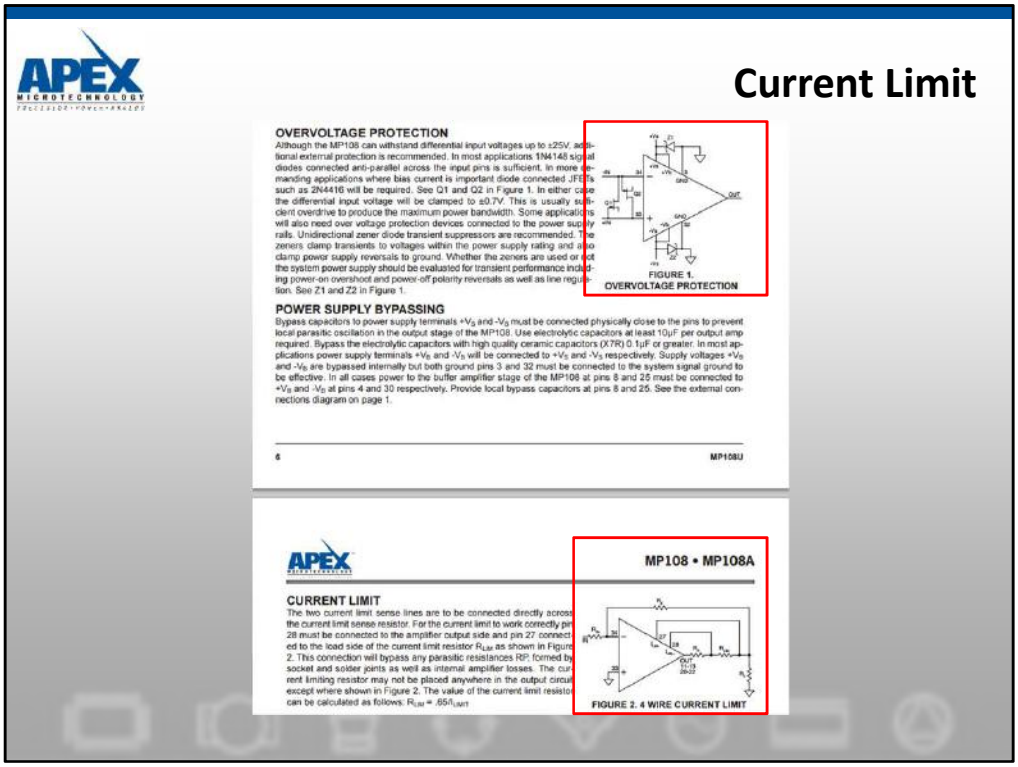
A way to force output voltage where ever needed to maintain constant output current.

- A non-linear mode of operation
- $V_{OUT} = ƒ(I_{LIMIT}$ and $Z_{LOAD})$
- I_{LIMIT} is only one term of the power equation

Current limit circuits do what their name implies but they are not magic cures for all load fault conditions. The non-linear operation (the op amp is unable to satisfy input signal/feedback demands) means monitoring the inputs for the presence of a differential voltage will signal this mode of operation.

Usually the current limit mode will reduce the output voltage but this is not always true. To determine critical survival the worst case voltage stress across the conducting transistor must be determined.

Current Limit



OVERVOLTAGE PROTECTION

Although the MP108 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

FIGURE 1. OVERVOLTAGE PROTECTION

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP108. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. In most applications power supply terminals $+V_S$ and $-V_S$ will be connected to $+V_S$ and $-V_S$ respectively. Supply voltages $+V_S$ and $-V_S$ are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP108 at pins 8 and 25 must be connected to $+V_S$ and $-V_S$ at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See the external connections diagram on page 1.

6 MP108U

MP108 • MP108A

CURRENT LIMIT

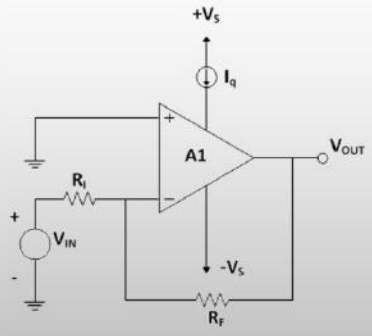
The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances RP, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

FIGURE 2. 4 WIRE CURRENT LIMIT

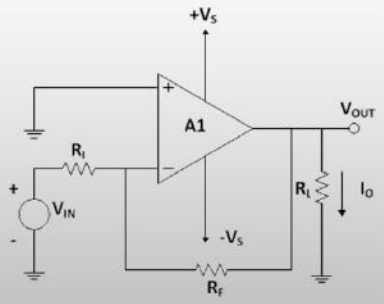
There are several different internal schemes used to implement current limit in Apex products. Most datasheets will have a formula or some text explaining the implementation used for the product. If there is no formula or reference, refer to application note 1.

Note that in most cases, all of the output current flows through the current limit resistor. Use $I^2 * R$ to determine the power rating for the resistor

Power Op Amp "DC Power Dissipation"



$Pd_q = [+V_s - (-V_s)][I_q]$



$Pd_{out} = (+V_s - V_o)Io$

$Pd_{out}(max) = [1/2\ V_s][I_o]$

$Pd_{out}(max) = \frac{V_s^2}{4RL}$

$Pd_{total} = Pd_q + Pd_{out}$

When calculating power dissipation in an amplifier, you MUST NOT FORGET THAT POWER DISSIPATION IN THE AMPLIFIER IS NOT EQUAL TO POWER DISSIPATION IN THE LOAD. That is, most of the time. One exception is when the output voltage is half of the supply voltage and the load is resistive. In this particular case the power dissipations are equal.

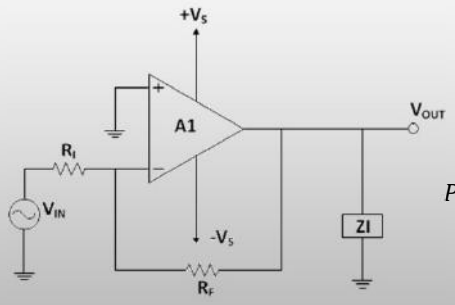
Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple.

The first portion of power dissipation is due to the quiescent power that the amplifier dissipates simply by sitting there with +Vs and –Vs applied. Multiplying total supply voltage by quiescent current gives the value of this power dissipation.

The maximum power dissipation in the amplifier under DC conditions with a resistive load is when the output voltage is 1/2 of the supply voltage. Therefore, whatever current is delivered to the load at 1/2 supply voltage multiplied by 1/2 supply voltage gives maximum power dissipation in the amplifier. The total dissipation is the sum of these two.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

Power Op Amp “AC Power Dissipation”



$$ZL = |Z_l|$$

$$Pd_{out}(max) = \frac{2V_s^2}{\pi^2 ZL \cos\theta}, \quad \theta < 40°$$

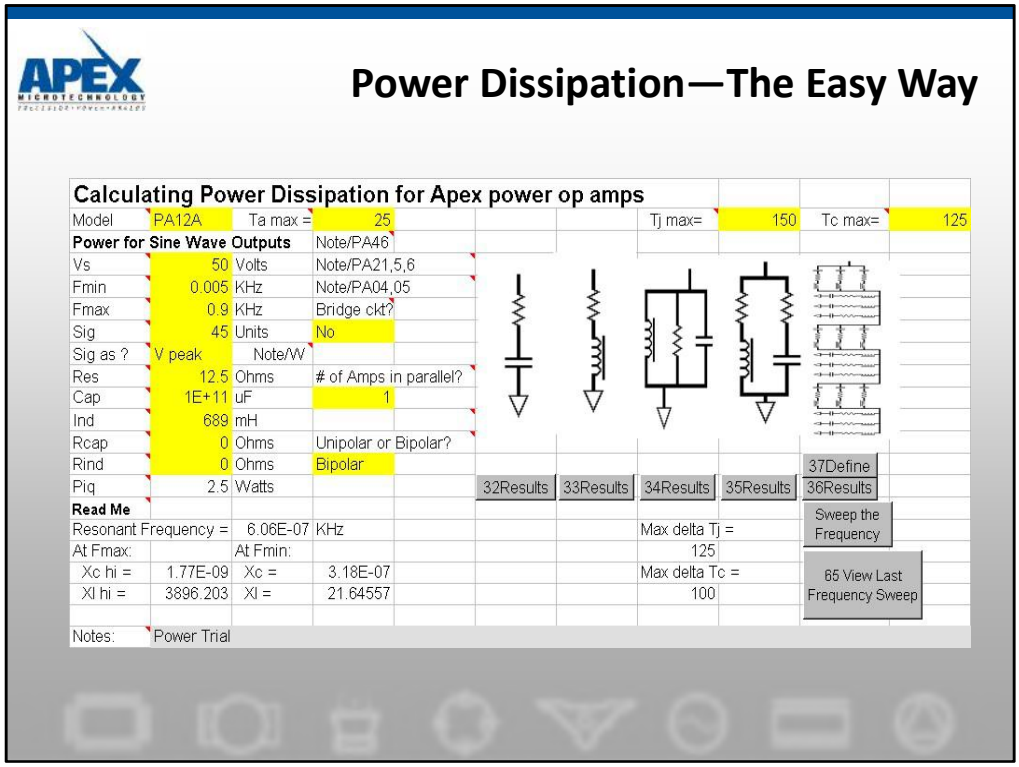
$$Pd_{out}(max) = \frac{V_S 2}{2ZL}\left[\frac{4}{\pi} - Cos\theta\right], \quad \theta > 40°$$

$$P_{total} = Pd_{out}(max) + Pd_q$$

With an AC output and/or reactive loads, output power dissipation calculations can get a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements. Both Application Note 22 and Application Note 1 General Operating Considerations give details on measuring AC power dissipation.

Worst case AC power dissipation formulae are given above for any reactive load range. With these worst case formulae one can calculate worst case power dissipation in the output stage for AC drive conditions and reactive loads.For most power op amps output stage power dissipation is the dominant component of total power dissipation so adding worst case AC output power dissipation with DC quiescent power dissipation and using AC Rθjc AC thermal
impedance for junction to case, will be sufficient for heatsink calculations.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

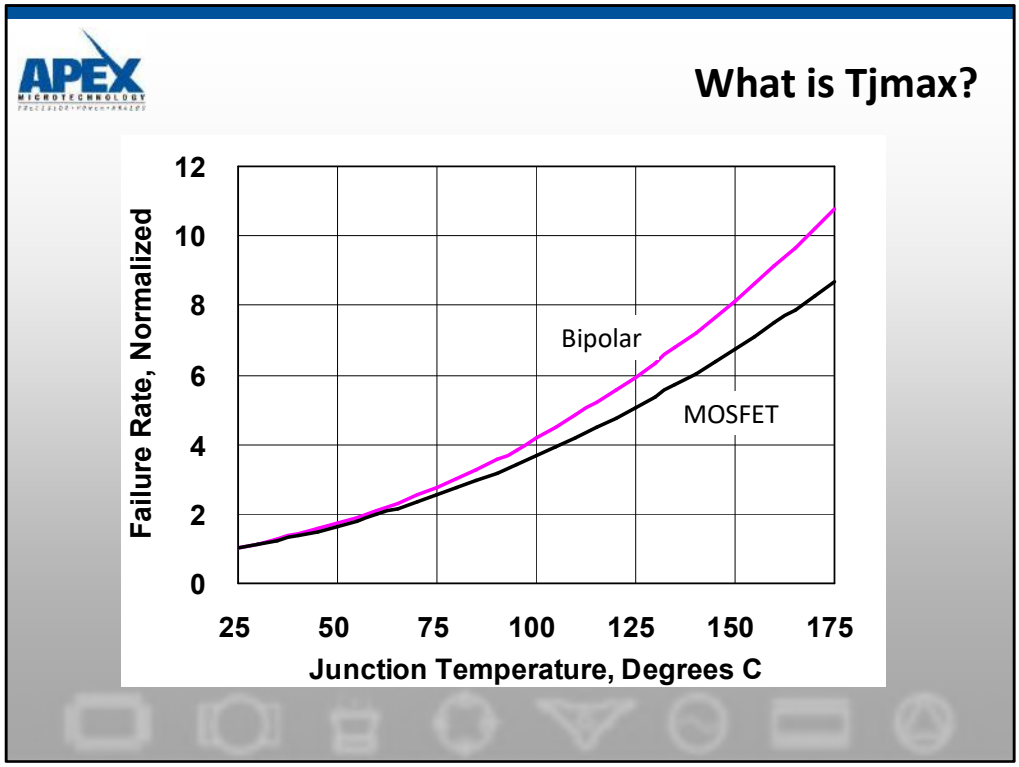


If your application can be modeled as a sine wave of any frequency, this sheet will tell you a lot. Entering a model pulls up a sizable portion of the data sheet for calculation and flag raising. Enter the three temperatures: ambient from the application, case per data sheet max or lower, and junction per contract or philosophy on reliability. If you need DC response, anything below 60Hz is OK. Define your output signal in terms of volts, amps or watts. If your load can be modeled by one of the first four diagrams, enter the values below. If you need diagram 5, use the Define Load command button.

Be sure to check these three cells!
If the Bridge circuit cell is “Yes”, the signal and load values specified will be treated as total but internal power will be for a single op amp.
Internal power will be divided by the # of parallel amplifiers.
“Unipolar” forces only one power supply and the use of DC thermal resistance.

A few useful pieces of information show up on this screen along with a red flag if your specified supply voltage is out of bounds. For more answers use the command button below the desired load diagram.

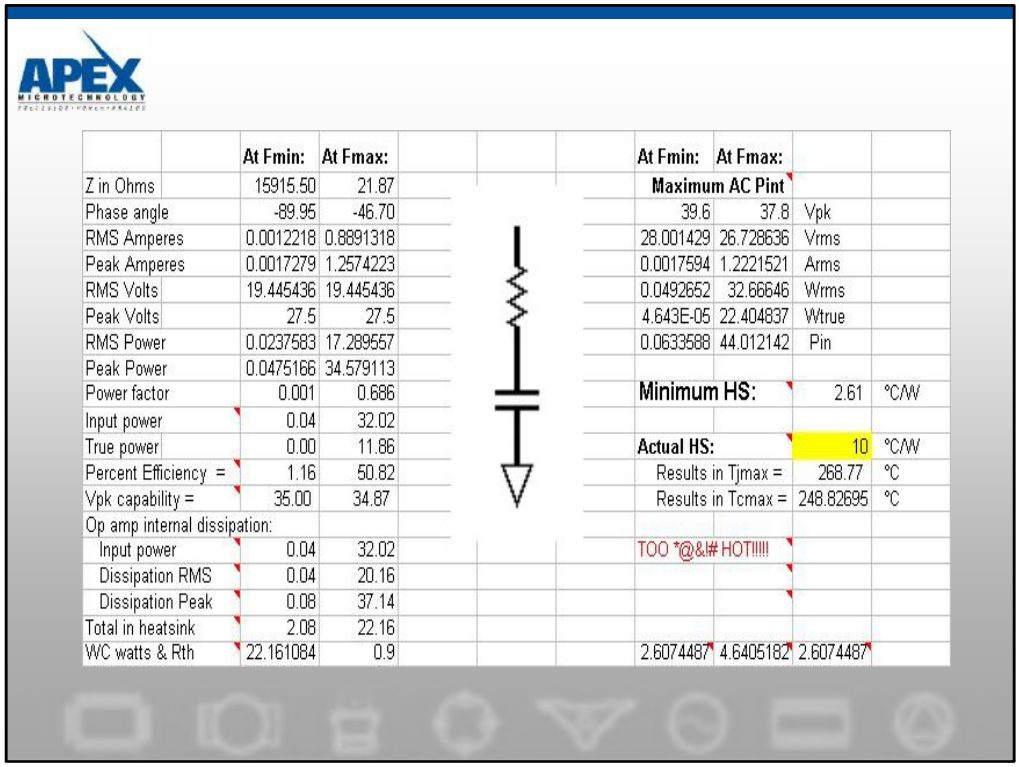
Ref. AN37



While this author would be the first to agree MIL-HDBK-217 has a few quirks and is very often misused, it does have the curves sloping in the right direction. Electronics is similar to your car, toaster- -almost anything, even engineers! Run it too hot and it dies an early death. Apex suggests a maximum of 150°C for normal commercial applications. If the equipment is remotely located or down time is extremely expensive a lower temperature is appropriate.

This graph represents the temperature acceleration factors from revision F, Notice 2.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING



	At Fmin:	At Fmax:		At Fmin:	At Fmax:		
Z in Ohms	15915.50	21.87		Maximum AC Pint			
Phase angle	-89.95	-46.70		39.6	37.8	Vpk	
RMS Amperes	0.0012218	0.8891318		28.001429	26.728636	Vrms	
Peak Amperes	0.0017279	1.2574223		0.0017594	1.2221521	Arms	
RMS Volts	19.445436	19.445436		0.0492652	32.66646	Wrms	
Peak Volts	27.5	27.5		4.643E-05	22.404837	Wtrue	
RMS Power	0.0237583	17.289557		0.0633588	44.012142	Pin	
Peak Power	0.0475166	34.579113					
Power factor	0.001	0.686		Minimum HS:		2.61	°C/W
Input power	0.04	32.02					
True power	0.00	11.86		Actual HS:		10	°C/W
Percent Efficiency =	1.16	50.82		Results in Tjmax =		268.77	°C
Vpk capability =	35.00	34.87		Results in Tcmax =		248.82695	°C
Op amp internal dissipation:							
Input power	0.04	32.02		TOO *@&!# HOT!!!!			
Dissipation RMS	0.04	20.16					
Dissipation Peak	0.08	37.14					
Total in heatsink	2.08	22.16					
WC watts & Rth	22.161084	0.9		2.6074487	4.6405182	2.6074487	

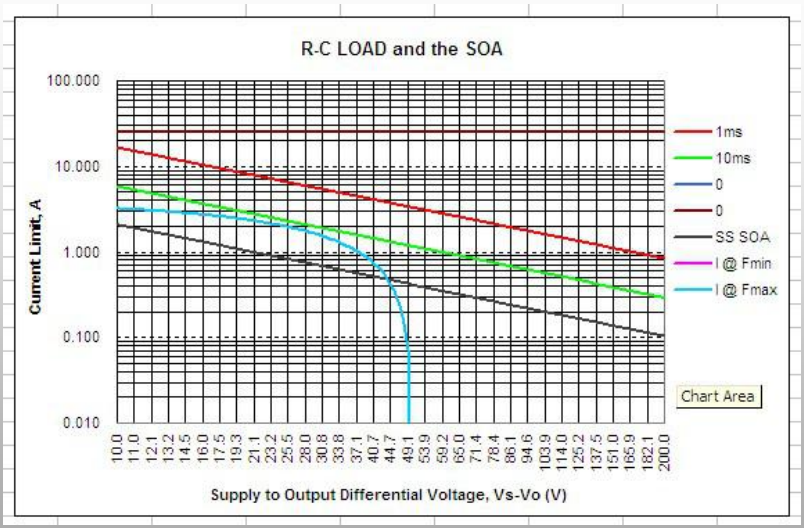
If you're in a hurry, go to the right side just above the yellow box to find the smallest heatsink usable. Enter data sheet rating for selected heatsink to see maximum case and junction temperatures.

Since the low frequency load is so light we'll look at the high frequency numbers only. Below impedance & angle are the operating points of the load; amps, volts, watts and power factor. Next we find power being drawn from the supplies due to driving the load and true power dissipated by the load. This leads to efficiency (at your specified signal level). If the peak output capability based on the supply and output current is more than a few volts above required output, lowering supplies will reduce internal dissipation.

In the upper right, the worst case amplitude for your load is estimated (this amplitude varies with phase angle). Op amp RMS dissipation is calculated by subtracting true power from input power at worst case amplitude or your maximum level. Peak op amp dissipation is taken from the graph below. "Total in heatsink" uses peak if the frequency is below 60Hz (else RMS), then adds quiescent power. The last line picks worst case frequency and gives you power and thermal resistance for heatsink sizing. The three cells in the lower right are heatsink needed to keep the case cool, to keep the junctions cool without regard to the case, and the smaller of the two.

Ref. AN37

R-C Load and the SOA



Remember transistor load lines from school? This is it and there should be no major surprises. At least none that we can't explain or fix.

The lack of an Fmin curve in this example is because our load is completely off scale with peak current of only 1.7mA.

Note the 10ms and 1ms pulse lines. For the conditions shown above, a 10ms puls at 10% duty cycle or less would be safe. Longer pulses or continuous duty would violate the SOA and would result in the creation of an expensive paper weight.

If one of the load lines peaks over the SOA curve remember we are looking at ½ of a sine wave while the heatsink may have been sized on RMS values. If it looks like you have a lot of wasted power handling capability, go back and enter maximum case and junction temperatures calculated for the actual heatsink to be used.

Application note 37 describes the use of the PowerDesign spreadsheet tool to aid the designer in calculating load lines and determining the suitability of the product.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22, AN37

Resistive Load Line Calculations

PA07

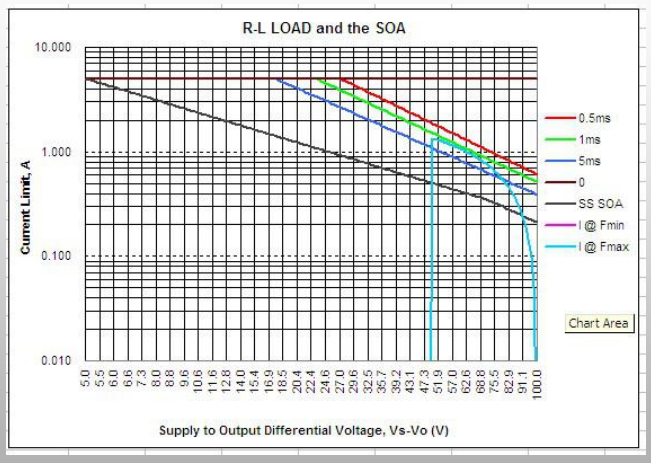
100Vs

37.3 Ω

1.34A @ 50V

67 W max

But…



So, you've checked the maximum power dissipation at ½ the single supply voltage and all is well (discounting the fact this example requires an infinite heatsink). The job is not over! At frequencies below 60Hz you do not to cross the second breakdown curve at all. At higher frequencies, keeping the duty cycle of these excursions down to 5% will keep you out of trouble.

When using dual symmetric supplies and pure resistive loads, all Apex power op amps are immune to this problem. For all other cases use Power Design.xls to plot sine wave load lines for you. This graph is from the power sheet but a trick had to be pulled to get a plot where output voltage is over 50% of the total supply voltage. In the Vs cell enter 100 volts and use the Unipolar or Bipolar input cell to specify Unipolar output current. This causes Power Design to calculate quiescent current on a single 100V supply and to use DC thermal resistance because only one transistor is doing all the work.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING, AN22

Typical Load Line Calculations

PA12

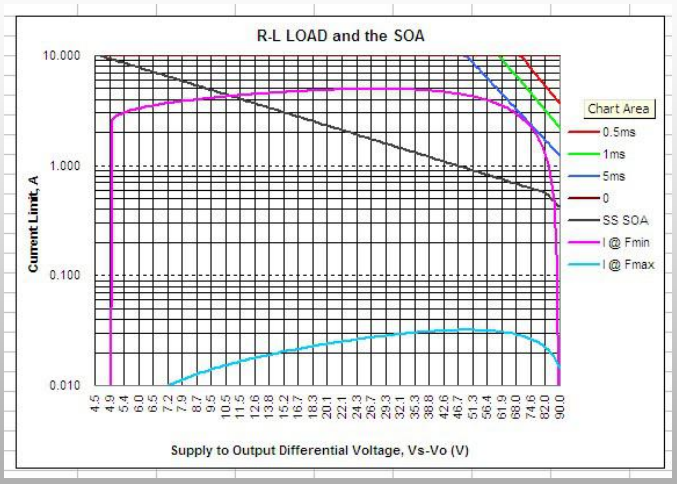
±50Vs

45Vpk @ 5A

9Ω @ 60°

112VA→Load

But…



Can a 125W, 10A device drive this 5A load? It's a large coil (250mH and 4.5Ω) and the frequency is only 5Hz. If efficiency were only 50%, delivering this 112VA to the load should be OK, shouldn't it? No. And no.

Phase shift is the killer here. You can see right away the load line exceeds the second breakdown curve. Look at current at the 56.2V stress level; its almost 4A (3.93 actually) giving peak dissipation of about 220W. Indeed, the data above this graph says the number is 223.5W (including Iq). We are in big trouble even though a 9Ω pure resistive load would have been fine with dissipation of only 72W and no hint of second breakdown problems.

It is time to look for a bigger amplifier or negotiate the load specifications.

Typical Load Line Calculations

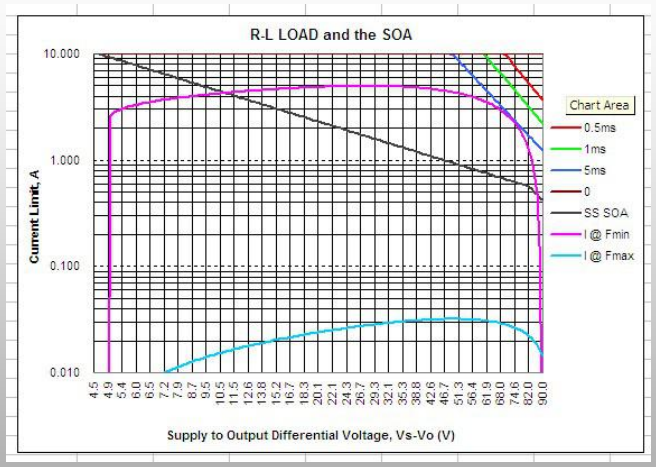
PA12

±50Vs

45Vpk @ 1.8A

30Ω @ 60°

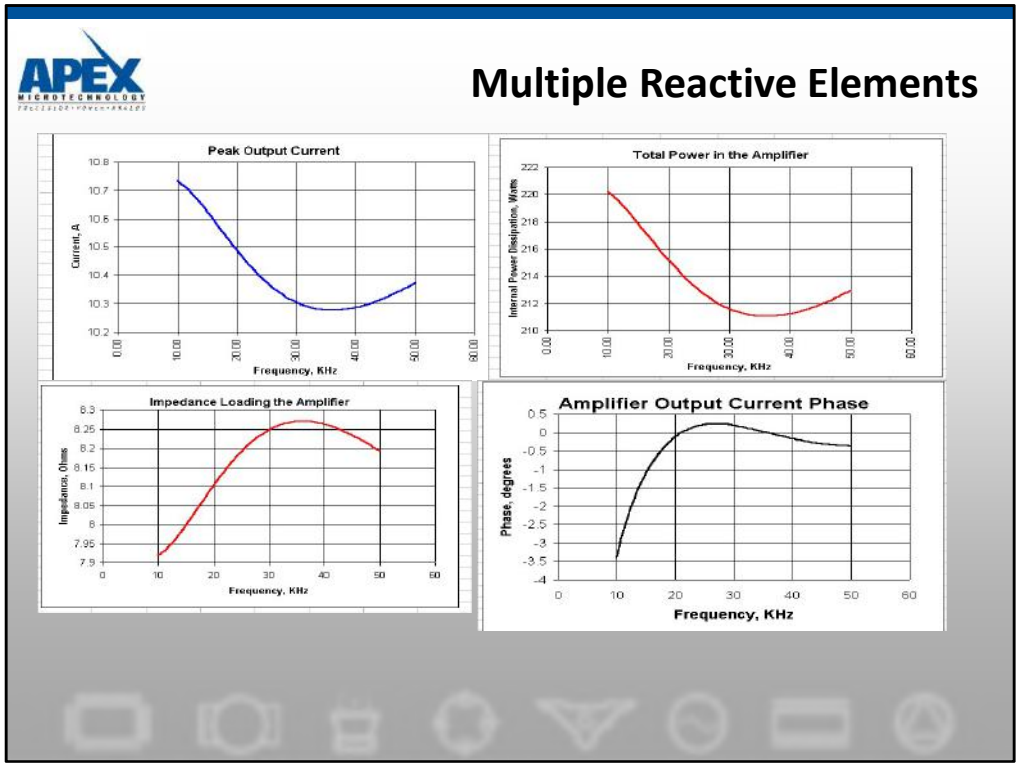
35VA→Load



Reducing the load requirements all the way to 30Ω produces a load line not in violation of the second breakdown curve and power dissipation in the amplifier is down to a manageable 72W.

The probability of negotiating load specs this far is rather dim. Its time to look at a bigger amplifier such as the PA05.

Of course, this is a very low frequency application with an inductive load so a switching amplifier such as the SA60 may be a much more suitable choice. The PWM section of the seminar explains the pros (high efficiency) and cons (high noise, more involved design) of using the switching amplifier approach.

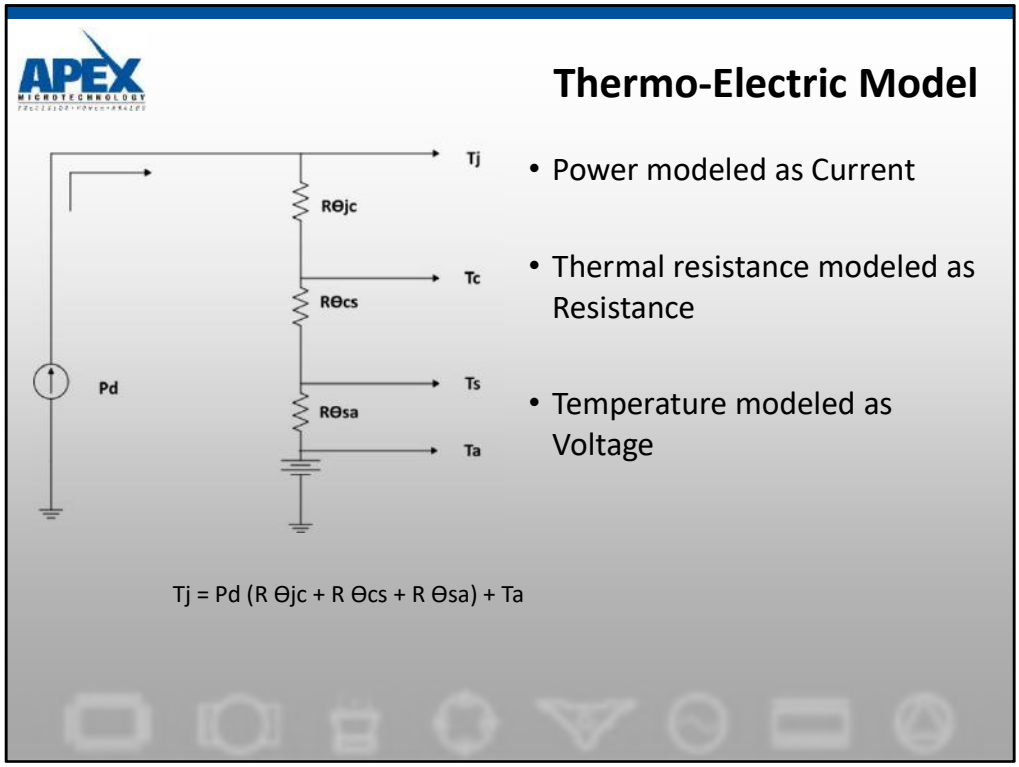


Any time an application has more than one reactive element, peak values of voltage, current, phase shift and power dissipation may not be at the minimum or maximum frequencies. It would be a good idea to run a frequency sweep to locate worst case operating points.

These graphs model operation of a tuned piezo load and the transmission line. In this case we find worst case power dissipation in the amplifier is at minimum frequency. Don't get caught by surprise with a complex load producing a power peak instead of a dip.

Frequency sweep requires Analysis ToolPak. If you see cells with #NAME? or a runtime error, try TOOLS, ADD-INS, Analysis ToolPak and then sweep.

Ref. AN37



The thermo-electric model translates power terms into their electrical equivalent. In this model, power is modeled as current, temperature is modeled as voltage, and thermal resistance is modeled as electrical resistance.

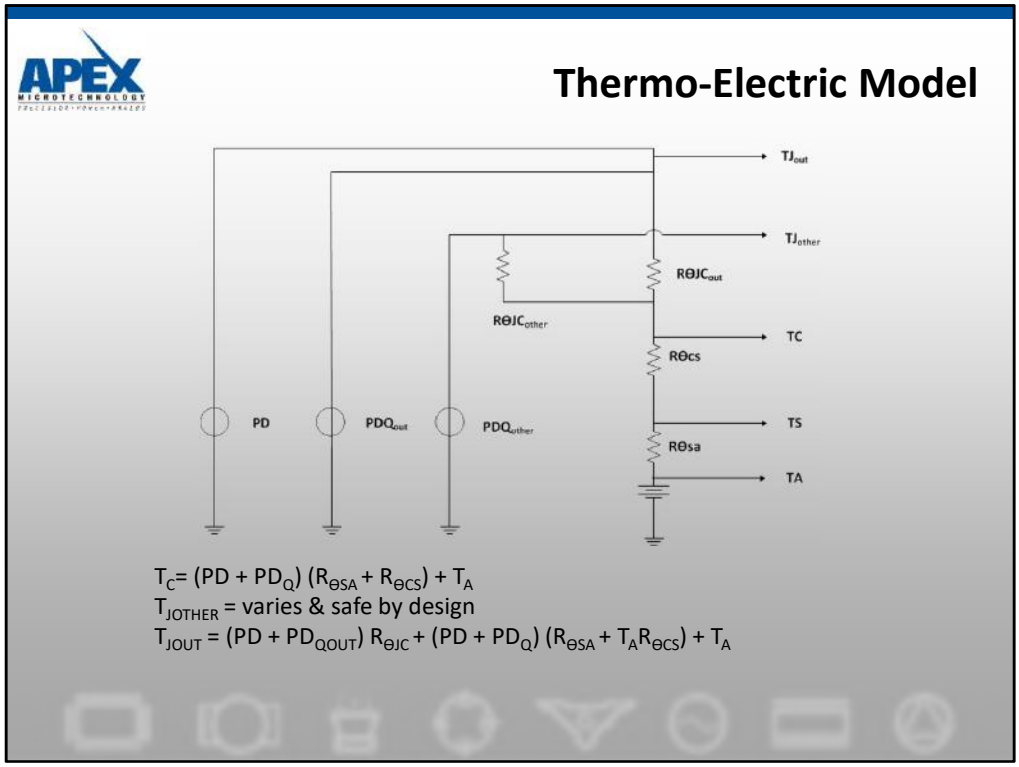
The real "name of the game" for power amplifiers is to keep Tj as low as possible. As you can see from the model, there are two approaches to doing this. The first is to reduce the current, ie; the power dissipation. The second is to reduce the thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the Vs-Vo quantity to as low a value as possible.

The thermal resistance problem should be attacked on all three fronts. Rjc, the thermal path resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a Rjc as affordable.

Rcs is the thermal resistance from the case to a heat sink. This resistance is minimized by good mounting techniques such as using thermally conductive grease or an approved thermal washer, properly torqueing the package, and by not using insulation washers.

The last piece of the thermal budget is Rsa, the thermal resistance of the heat sink to ambient air. This is a very crucial piece of the puzzle and should not be skimped on. A quick glance at an SOA curve that shows the difference between the power limitations of an amplifier with a 25°C case and an 85°C case shows the benefit of using the maximum heat sink allowable.
Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING



In this model, quiescent power has been split according to the actual transistors generating the heat. PDQout is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case PDQout.

PDQout = IQout (+VS + |-VS |)

PDQother is the current flowing in all the other components and could be found by subtracting PDQout from PDQ .

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum "Meets full range specifications" case temperature.

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:
1) Buy an amplifier with the lowest possible RØJC.
2) Use good mounting practices.
3) Use the largest practical heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

Heatsink Selection

PA02 POWER OP AMP

- P_d = 14 Watts
- T_a = 35° C
- R_{jc} = 2.6° C/W
- R_{cs} = .2° C/W

APEX HEATSINK TO KEEP T_j = 100° C

- $T_j = P_d (R_{jc} + R_{cs} + R_{sa}) + T_a$
- $100°C = 14W(2.6°C/W + .2°C/W + R_{sa}) + 35°C$
- R_{sa} = 1.8° C/W

SELECT APEX HS03:R_{sa} = 1.7° C/W

This calculation illustrates the heat sink selection procedure using the thermal electric model discussed. First we calculate the power dissipation within the amplifier under worst case conditions. In this example, that number came out to 14 watts. Next we pick a desired value of Tj. In this example, we picked a very conservative value of 100°C. This value of Tj will result in a very large mean time to failure, spelling reliability for this application. Consulting the data sheet for the PA02, we find that the maximum DC thermal resistance from junction to case is 2.6° C per watt. Next, we consult the APEX Data Book to determine that the typical case to heatsink resistance is between .1 and .2° C per watt, when thermal grease is used. Solving the given formula for the unknown, Rsa, we find that the required thermal resistance is less than or equal to 1.8° C per watt. This can easily be achieved by using the Apex HSO3 Heatsink which has an RSA of 1.7° C per watt.

If a system has forced air or a liquid cooling system available, physical size of the heatsink can be decreased. Heatsink data sheets often graph thermal resistance vs. air velocity. Fan data sheets usually speak of volume moved. At the very least a conversion is needed which takes in account the square area of the air path as it passes the heatsink.

Ref. AN1 INTERNAL POWER DISSIPATION AND HEATSINKING

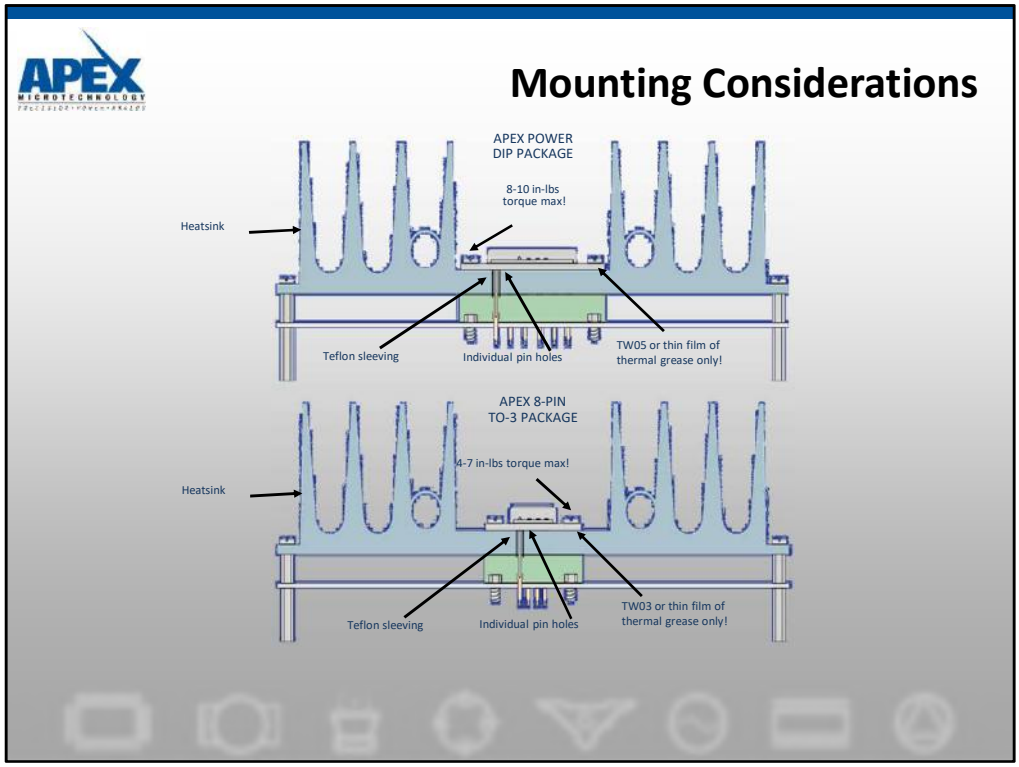
Thermal Capacity can be a Big Friend

- For pulse mode operation
- When pulses > 8ms
- Ap Note 11 Thermal Techniques
- Thermal response ≅ to R-C response

- $\Delta V = e^{x}\text{-}t / RC$
- Δ temp = e^{x}-t / TAU

If the drive signal is pulse mode, internal power between pulses is zero and individual pulses are less than 8ms, size the heatsink by dividing the pulse power by the duty cycle and adding the quiescent power.

For other pulse mode operations Application Note 11, Thermal Techniques, is the reference. It will explain how to calculate thermal capacity, thermal time constants and plot the charge/discharge curve. It also lists some common unit conversions and constants.



Key areas to check for proper mounting techniques:

1) Heatsink flatness.

2) Individual heatsink thru-holes for each pin.

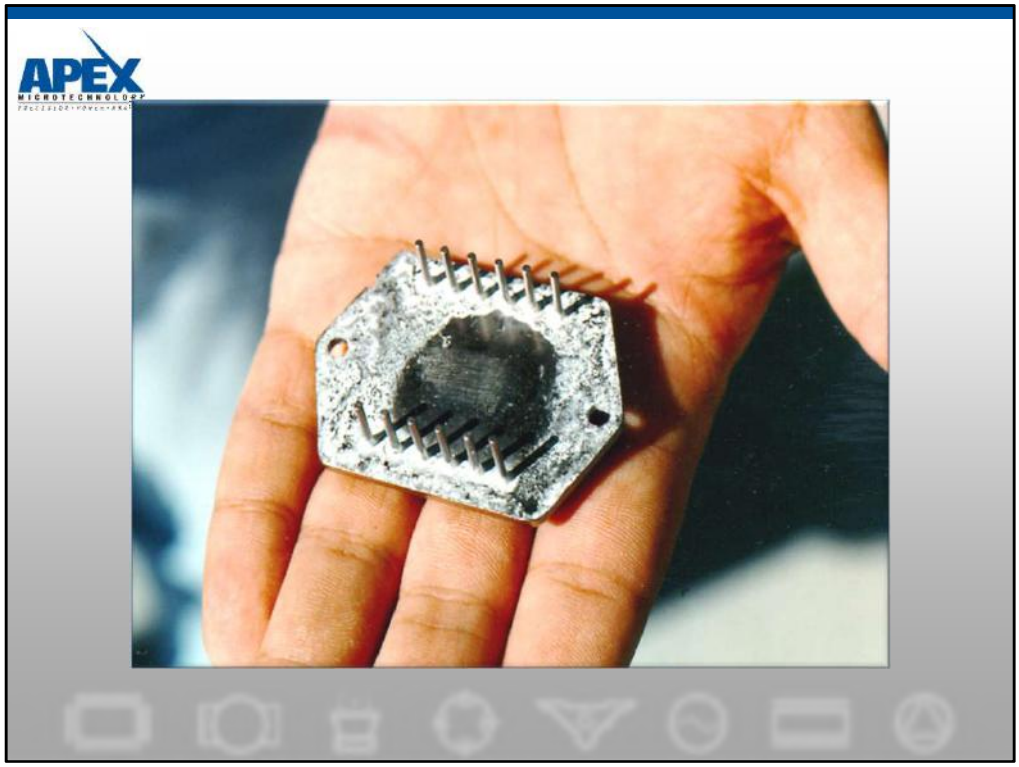
3) Thermal interface between case and heatsink.

4) Mounting torque.

5) Sleeving on pins—thickness of heatsink.

A detailed discussion of these areas follows.

Ref. AN1 AMPLIFIER MOUNTING AND MECHANCIAL CONSIDERATIONS

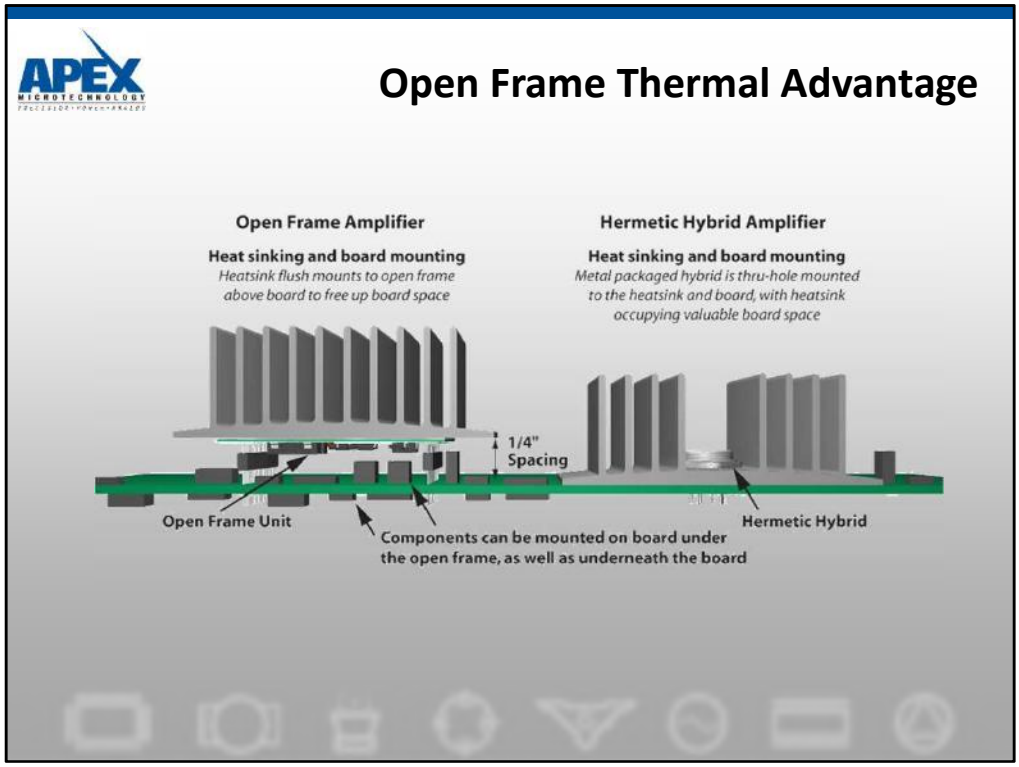


Properly applied grease results in good thermal performance. The operator variable shown above leaves the central area (where the heat is developed) with a high thermal path which led to amplifier destruction. Another variable to watch for is separation of the liquid from the solids in the grease. Too high a percentage of either can result in amplifier destruction due to thermal or mechanical stress. Buying thermal grease in a can or jar rather than a tube allows stiring to avoid the separation problem.

This slide also introduces the Apex failure analysis service. If you have a an elusive problem, call us. We'll attempt to solve it over the phone. Its always good to have a schematic handy you can fax. If appropriate, we'll give you an RMA (return material authorization) to start a failure analysis. We will:

1. Perform an external visual examination.
2. Test the part to all room temperature electrical specifications.
3. Delid and perform an internal visual.
4. Trouble shoot the circuit.

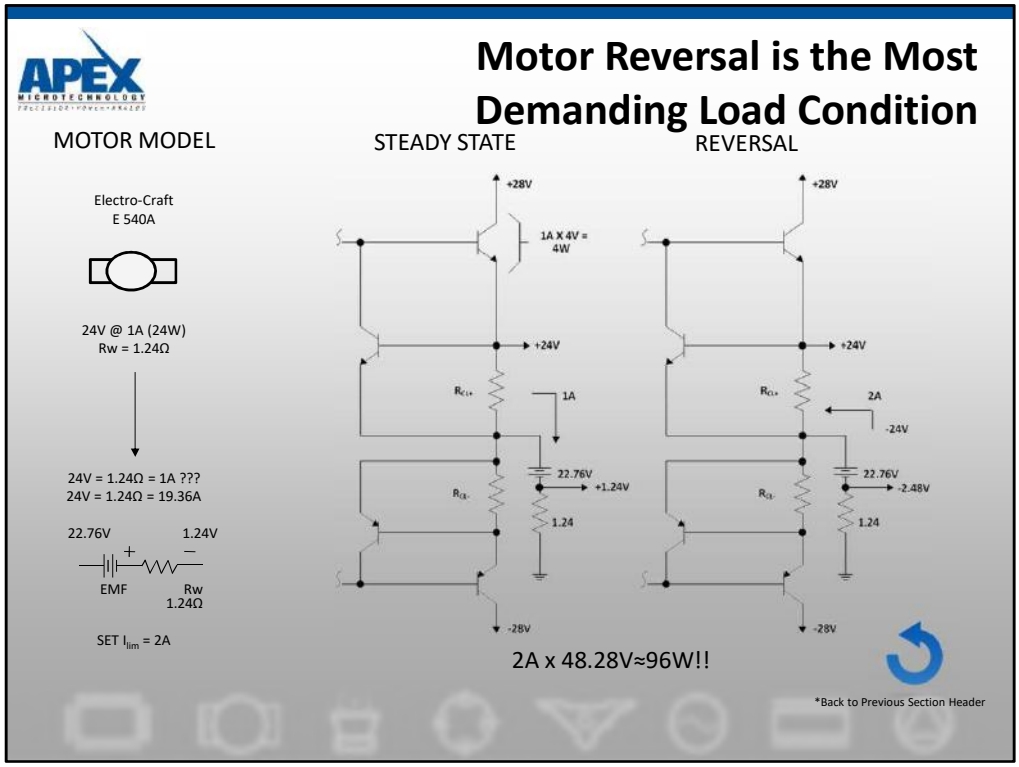
Many times the physical evidence helps pinpoint the problem. The location and nature of damage usually yields a suggestion on how to eliminate the problem.



With the Open Frame packaging style, there are significant thermal and mechanical advantages. Because the entire back side of the open frame is thermally conductive aluminum, any flat backed heatsink will do. We do not need to machine away the fins in order to accommodate the amplifier and there are no precision holes necessary for the pins to feed through.

Because the package of the open frame is larger, the thermal flux density of the heatsink can be reduced. In all, a smaller, lighter, and less expensive heatsink can be used with an Open Frame product compared to a hybrid with the same power dissipation.

Ref: AN11



A DC motor driven at 24V with 1A steady state current flow and a winding resistance specified at 1.24Ω can be modeled as a resistor in series with an EMF. In this example since the 1A drops 1.24V across the 1.24Ω, the remaining 22.76V is back EMF.

Under steady state conditions the motor voltage of 24V subtracted from the supply voltage of 28V leaves a 4V drop across the conducting transistor and a power dissipation of 4W.

When the amplifier is told to reverse the motor, the output of the amplifier attempts to go to -24V. If it could do so this -24V would add to the EMF of 22.76V to give -46.76V across the 1.24Ω resistor, resulting in a current flow of 37.71A. No way! Current limit is set at 2A.

When the current limit value of 2A flows across the winding resistance it drops 2.48V. The positive 22.76V of EMF is added to this negative 2.48V to give an output voltage of 20.28V. The difference between the output and the negative supply is now 28 -(-20.28) or 48.28V. That stress voltage on the conducting transistor means that the internal dissipation in the amplifier immediately after reversal is 48.28 volts * 2 amps or 96.56 watts!

This shows that a simple reversal can increase instantaneous power dissipation in the amplifier by over an order of magnitude. Judicious setting of current limiting and slowing the electrical response time will optimize reliability and mechanical response time.

Ref. AN24