HIGH POWER TECHNIQUES

Dead Op Amps Don't Power Much

Who, me? Read the book?

- AN1 General Operating Considerations
- AN8 Optimizing Output Power
- AN9 Current Limiting
- AN19 Stability for Power Amplifiers
- AN25 Driving Capacitive Loads

- Subject Index

We've heard of the male stereotype character who reads directions only as a matter of last resort. This anonymous author isn't much of a reader but after a few explosions, I broke down and opened the book- -the Apex book of course.

Better than ¼ of the book is application notes, arranged mostly by type of application rather than amplifier model. This along with a comprehensive subject index make this book very valuable.

Here's my suggestion: Thumb through at least the Ap Notes above looking at pictures and paragraph titles. Then check out the index in the back.

Quiz for today: What is the Apex Cage Code?

The Bridge Circuit

- Double the voltage swing
- Double the slew rate
- Double the power

- Bipolar drive on a single supply
- More efficient use of supplies

There are two basic categories of motivation to use the bridge circuit. The most common is doubling the voltage capability of the whole line of power op amps. The second category solves some limited supply availability situations.

Bridge Basics

Primary
$V_{OUT} = X$
$I_{LIMIT} = Y$

Follower
$V_{OUT} = -X$
$I_{LIMIT} = 1.2Y$

The primary amplifier in the bridge may be configured in any manner suitable for a single version of the particular model. Set gain of the primary for ½ the total required to drive the load. The follower provides the other half of the gain by inverting the output of the primary and driving the opposite terminal of the load. Dual supply operation is the easiest but asymmetric or single supply versions are also common.

The R-C network is often used to fool the follower amplifier into believing it is running at the same gain as the primary. This is important when using externally compensated amplifiers at other than their lowest bandwidth compensation. Set Rn for Rin||Rn = Rf/gain of the primary. Set Cn for a corner frequency with Rn at least 1½ decades below unity gain bandwidth.

Consider a shorted load. Tolerances make it impossible to set identical current limits on the primary and the follower; one will go into current limit, the other will never reach the limiting level. Assume the primary limits and the follower reduces its drive to the load also because it is still in a linear inverting mode. With both amplifier outputs going toward zero, power dissipations are equal and worst case is Ilimit * ½ total supply.

If the follower limits first, the primary remains linear and capable of driving to either rail leaving a power stress on the follower of Ilimit * total supply.

Ref. AN20
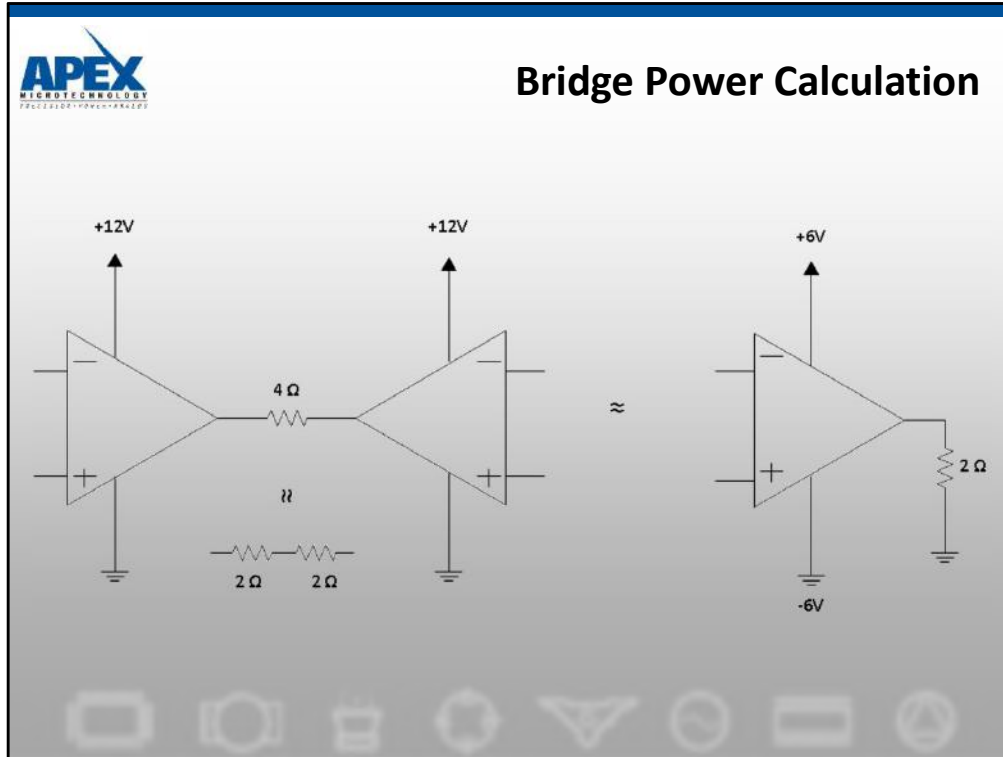
There are several formulae available for calculating worst case power dissipation in a power amplifier (refer to APEX catalog "General Operating Considerations" as well as previous seminar text). These formulae are based on a single power op amp using bipolar, symmetrical supplies. But what about this single supply bridge?

Instead of attempting algebraic manipulation of the formulas, try using circuit algebra. Knowing the primary and follower drive equally but in opposite directions tells us the ohmic center of the load does not move. This leads to an equivalent two resistor load where the center voltage can be calculated. When using dual symmetric supplies the center is almost always ground and we have an equivalent circuit right away.

For the single supply the center of the equivalent load is almost always the mid-point of the supply. Simply lowering all voltages by the load center voltage yields the same equivalent circuit. Simply calculate power dissipation of the equivalent and don't forget to double this figure.

If you are using Power Design you will need the voltage translation portion of this exercise, but not the equivalent load. Enter the total load, total signal level and "Yes" in the bridge question yellow cell.

Ref. AN37

A Weird & Dangerous Bridge
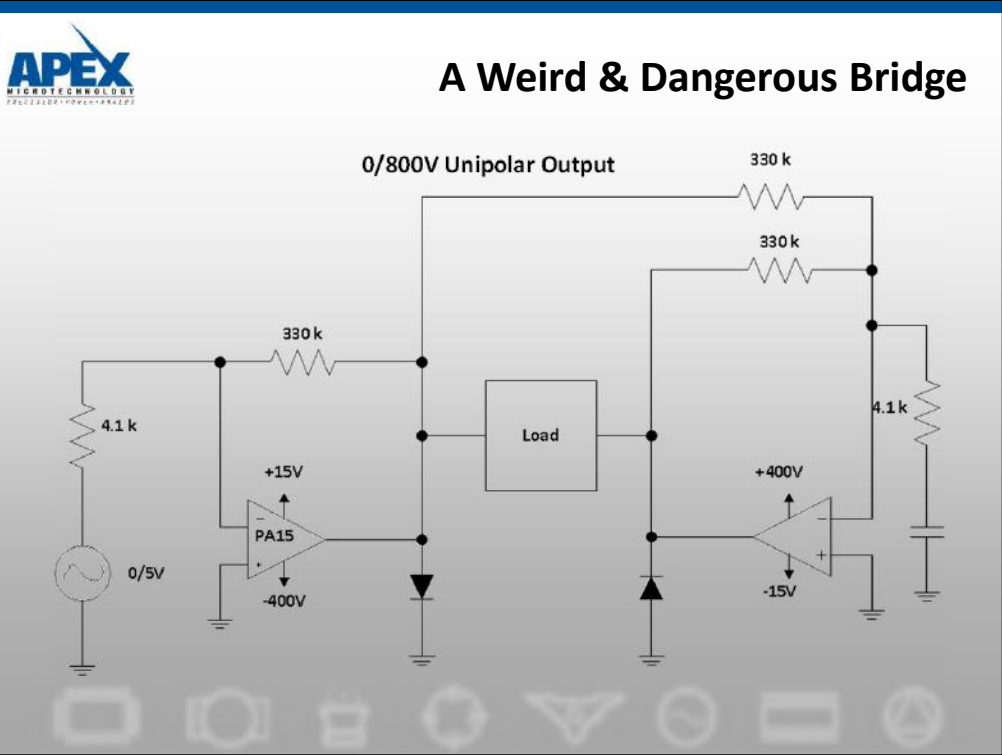
No, this is not the most common bridge circuit. But consider that the only other choice above 450V total supply is the PA89 which is quite slow and costs about $200 more than two PA15 amplifiers (both @ 100 quantity).

Dangerous? Any 800V circuit qualifies for this description but from the op amp point of view this one is a little more so because there are voltages in the area greater than his supply rails.

The left hand op amp swings 0 to -400V; the right hand from 0 to +400V. With the load looking at these two voltages differentially it sees 0/800V.

Consider a shorted load causing the right hand amplifier to current limit. If the left amplifier ever goes below -15V, he can destroy his partner. The diodes prevent this.

Ref. AN20 UNIPOLAR OUTPUT

Output Current Buffers

- Multiplies power & current capabilities

- Small loss of swing capability
- More prone to oscillate

Class C Current Buffer

Speed Limit Strictly Enforced

2.67 k   100 k

R$_{G+}$ 100   VN0335

+145V

2N2222   R$_{CL+}$ 0.47

PA241   R$_{CL}$ 330   R$_{GS}$ 1.1 k

INPUT

2.2 k   2N2907

10pF   R$_{CL-}$ 0.47

1N914

R$_{G-}$ 100   VPO335

-145V

No FET bias = No chance for thermal runaway
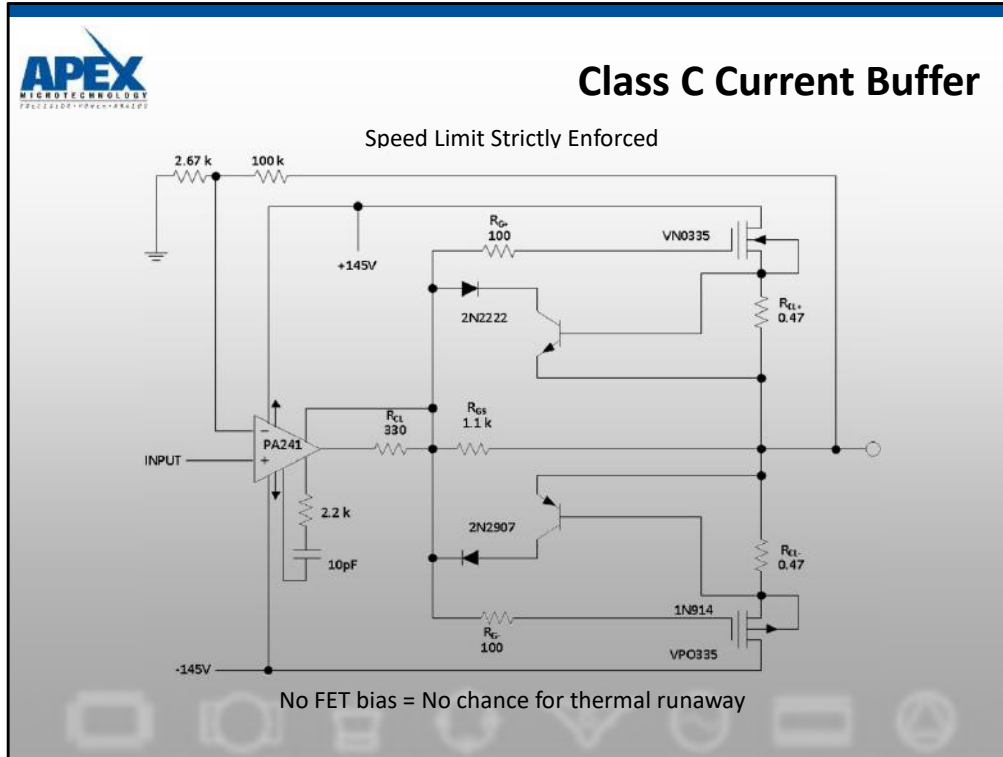
The choice of specific MOSFETs is determined entirely by current, voltage and power dissipation requirements. There are no radical differences among the different MOSFETs regarding threshold voltages of transconductance. Note that each MOSFET must be rated to handle the total supply voltage, 300V in this case.

Current limits work like the circuits we covered earlier. Power dissipation requirements for the MOSFETs can also be found with methods we learned earlier, just remember the power is split between the two packages if the signal is AC only. Power Design will calculate the watts, plug in the driver amplifier, the real load and ignore the red flags.

The 330 Ω current limit resistor sets the PA241 current limit to approximately 9mA. This current flowing across RGS limits drive voltage on the MOSFETs to 10V. This current also lowers crossover distortion. Worst case (during output stage current limit) power dissipation in the PA44 will then be 1.3W due to output current plus 0.6W due to quiescent current totaling 1.9W. Unless you are willing to cut holes in the PC board to to contact the bottom of the surface mount package with an air or liquid cooling system, this is about the limit. Typical operation will generate less than 1W in the op amp. Replacing Rgs will a 10 to 12V bi-directional zener will allow a cooler running op amp at the cost of increased distortion.

If more power is required than a single pair of MOSFETs can handle, additional MOSFETs may be added in parallel. Each device needs its own source resistor and gate resistor but the small signal current limit transistor and diode need not be duplicated. Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

Complimentary Mosfet Buffers
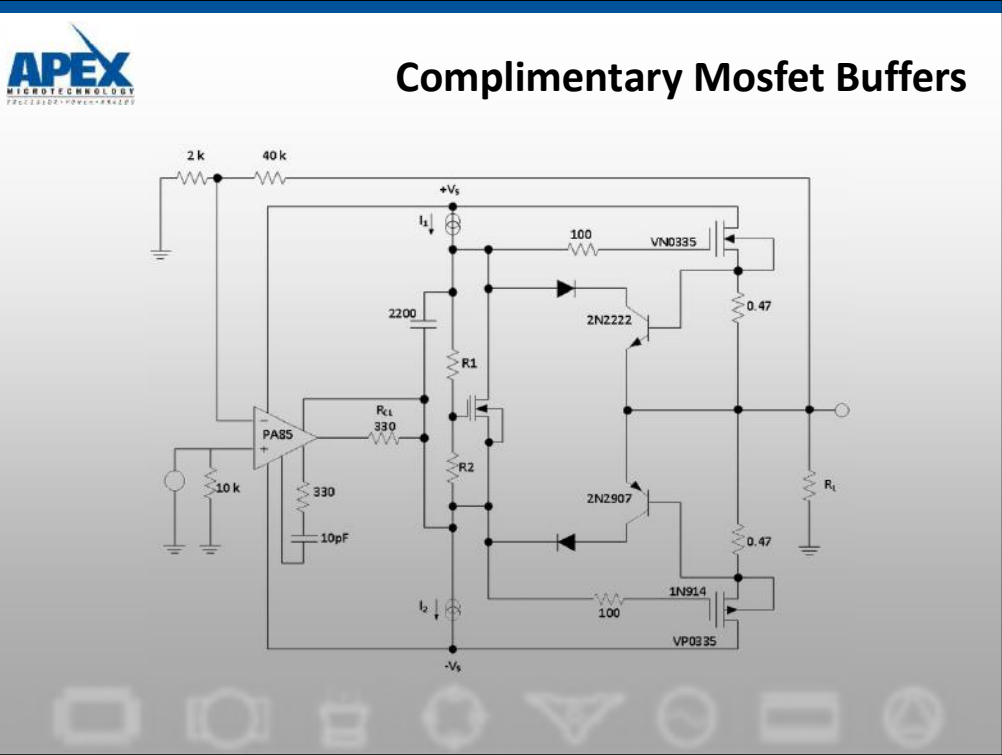
The class C circuit was able use a simplified version of this slide with no attempt to establish class A/B bias in the MOSFET output stage. In that circuit with no bias, the typical MOSFET threshold of 3V means the op amp must swing 6V during the crossover transition while the final output does not move. The additional circuitry used here will lower distortion and is increasingly important as frequency goes up. Distortion improvements better than an order of magnitude have been achieved.

As most power MOSFET data sheets provide little data on VGS variations at low currents over temperature, it facilitates the design process to have curve tracer data over the temperature range of interest. Design the VGS multiplier empirically. Current sources of 5mA and splitting the current equally between the resistors and the MOSFET area good starting points. Decreasing current in the MOSFET will increase the multiplier TC. Typical designs requiring low distortion will be set up to obtain 2mA or less bias in the output stage. The trade offs are more distortion with low current and danger of thermal runaway on the high end. Be absolutely sure to guardband your high end temperature. The circuit shown here is capable of distortion below .05% at 50KHz and is thermally stable (flat or negative TC of current in the output stage) over the range of -25°to 85°C.

Note that any multiplier voltage at all reduces distortion. Successful designs have even reduced the multiplier circuit to just a diode connected MOSFET. Do NOT use bipolar transistors or diodes for this biasing. Their TCs do not match those of the MOSFETs.

The 100Ω gate resistors prevent local output stage oscillations. It is important they be physically close to the MOSFETs. Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

Quasi-Complimentary Mosfet Buffers
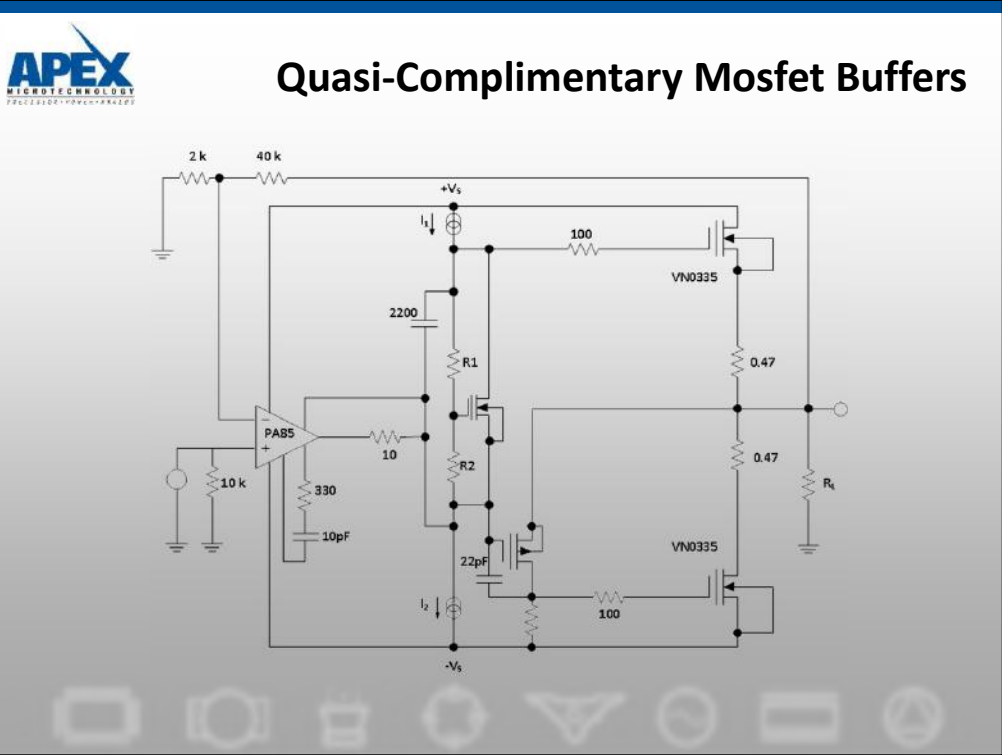
Above 300V p-channel high power MOSFETs can be difficult to find. An alternative is to use a quasi-complementary connection on the negative side. Since the required gate drive voltage of the output device appears across RG, its value will set the maximum current through the p-channel MOSFET. Typical maximum gate drive requirements are 10V. This circuit has demonstrated a slew rate of 360V/µs. A second disadvantage of the quasi-complementary design is higher saturation voltage to the negative rail because two gate-source voltages are stacked between the rail and the output.

Connecting the op amp to the top side of the multiplier helps a little but both buffer design approaches can benefit from having the high voltage op amp operate on higher supply rails than the high power MOSFETs. This improves efficiency by allowing better saturation of the buffers.

Design criteria for the current sources, current limiters (not shown here) and multiplier are the same as with the complementary version. It is possible to omit one of the current sources in these circuits. However, this places an added heat burden on the high voltage op amp because the entire current of the remaining source must flow through it. When calculating this added dissipation, use the current and the total supply voltage. When both current sources are used the op amp need only make up the difference between them.

Ref. Use High-Voltage Op Amps to Drive Power MOSFETs, by Jerry Steele and Dennis Eddlemon, Electronic Design, June 24, 1993.

Parallel Op Amps

- Primary Op Amp in any configuration
- Follower Op Amp – unity gain buffer
- Use sharing resistors to reduce the effects of output difference errors (offset, phase lag, etc)
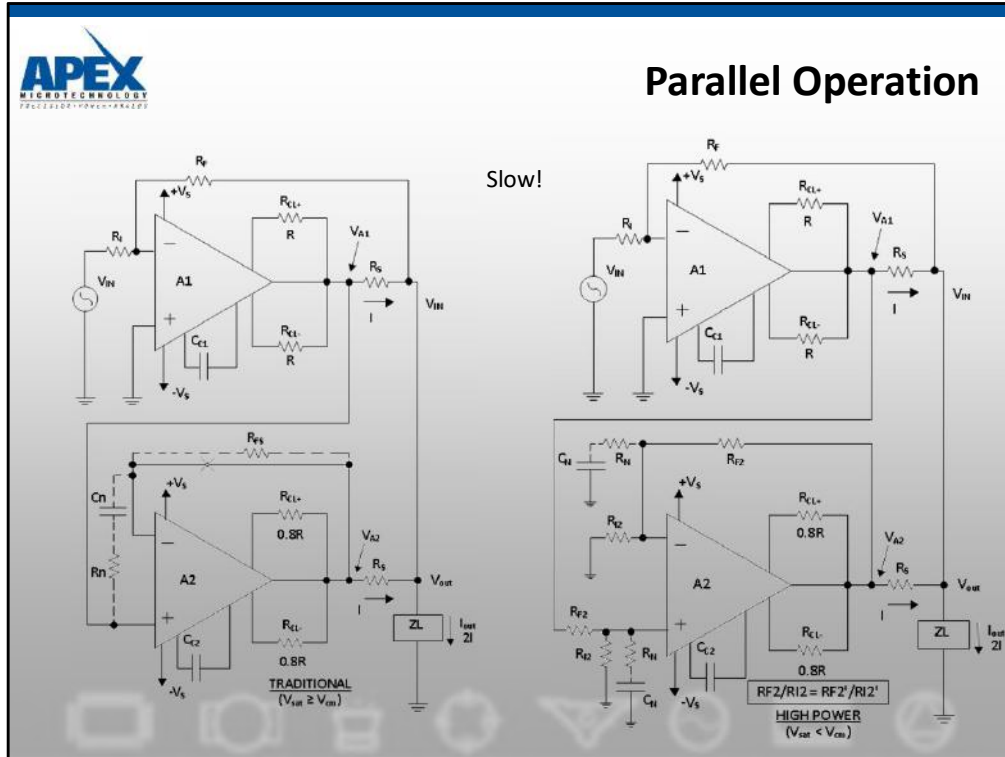
Occasionally it is desired to extend the SOA of a power op amp or provide higher currents to a load than the amplifier is capable of delivering on its own. Sometimes it is more cost effective to use power op amps in parallel rather than to select a larger power op amp.

The parallel power op amp circuit will consist of a primary amplifier, A1, which sets the Vout/Vin gain and follower amplifiers, A2 et al, which act as unity gain followers from the primary amplifier. For simplicity we will review the case of two power op amps in parallel.

We will need to consider the following key areas when paralleling power op amps:
1) Input offset voltage
2) Slew rate
3) Phase compensation
4) Current limit resistors

If we attempt to hook the outputs of two power op amps directly together the difference in input offset voltages, divided by theoretically zero ohms (a connecting wire), will cause huge circulating currents between the amplifiers, which will lead to rapid destruction. To minimize circulating currents we will need to add ballast resistors, Rs, as shown. The worst case circulating currents now are Icirc = Vos/2Rs. To minimize circulating currents we want Rs to be as large as possible. However, large values of Rs will add an additional voltage drop from the power supply rails and thereby reduce output voltage swing. Large values of Rs will also result in higher power dissipations. A rule of thumb compromise is to set Rs for circulating currents of about 1% of the maximum output current from each amplifier, .01I in our example.

Notice the particular arrangement of the primary and follower amplifiers. VA1 = IRs

+ Vout. However the point of feedback for A1 is at Vout causing A1 to control the gain for Vout/Vin. VA1 then becomes the input to A2. VA2 is then Vout + IRs. But Vout = VA1 – IRs. So each amplifier, A1 and A2, put out the same voltage across Rs and ZL and currents are thereby added to force 2I through the load with each amplifier providing one-half of the total.

The slew rates of A1 and A2 must be selected to be the same or A1 must be compensated for a lower slew rate. If A1 slews faster than A2, large circulating currents will result since A1 could be close to +Vs while A2 is still at zero output or worse near –Vs. Cc1 and Cc2 must then be selected to be the same or Cc1 greater than Cc2. Even with these steps for slew rate matching it is recommended to control the slew rate of Vin such that the amplifiers are not commanded to slew any faster than 50% – 75% of the selected slew rates. This is because, even with identical compensation, no two amplifiers will have identical slew rates.

If it is decided to have A2 not compensated for unity gain, to utilize a higher slew rate, use Noise Gain Compensation, shown by the dashed RFS and Rn, Cn combination, to compensate the amplifier for AC small signal stability.

Current limit resistors, Rcl+ and Rcl- for A2 should be 20% lower in value than currrent limit resistors for A1. This is to equalize SOA stresses during a fault condition. With the primary amplifier, A1, going into current limit first it will lower its output voltage thereby commanding A2 to do the same for equal sharing of stresses during a current limit induced condition.
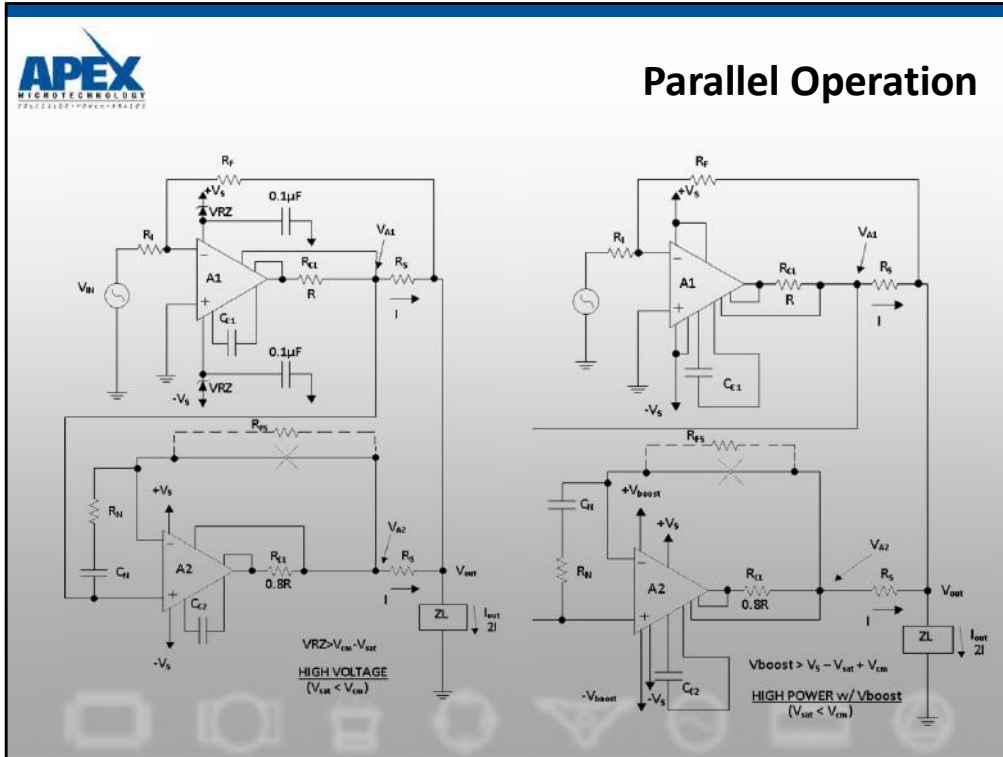
TRADITIONAL (Vsat ≥Vcm): This parallel configuration is for op amps whose saturation voltage is greater than or equal to their common mode voltage (Vsat Vcm). For example, a PA10 has a common mode voltage specification of +/- Vs-5 and a saturation voltage of +/- Vs -5. For the PA10 the output saturation voltage (5V) is equal to the common mode voltage (5V from either rail). We will not have any common mode voltage violation then if we drive the output of A1 into saturation as we will still be in compliance with the input common mode voltage specification for A2.

HIGH POWER (Vsat < Vcm): This parallel configuration is for amplifiers whose currents are greater than 200mA and whose saturation voltage is less than their common mode voltage (Vsat < Vcm).

For example, a PA02 has a common mode voltage specification of +/- Vs -6 and a saturation voltage of +/- Vs -2. For the PA02 the output saturation voltage (2V) is less than the common mode voltage (6V from either rail). If we drive the output of A1 directly into A2 in a unity gain voltage follower configuration we will have a common mode voltage violation.

The only way around this is to use a matched resistor network where the ratio of RF2/RI2 = RF2'/RI2'. The absolute value of each resistor is not as important as accurate ratio matching with temperature. If A1 and A2 are compensatible amplifiers and unity gain compensation is not desired, to use faster slew rates, then A1 can use noise gain compensation to guarantee AC small signal stability. Rn and Cn are our traditional Noise Gain Compensation components. Rn' and Cn' are essential to guarantee a flat Vout/Vin frequency response until we run out of loop gain.

Ref. AN26

Parallel Operation

All our previous "GENERAL COMMENTS" on the use of parallel power op amp circuits still apply to these configurations. Additional specific comments on each follows.

HIGH VOLTAGE (Vsat < Vcm):

This parallel configuration is for amplifiers whose currents are less than 200mA and whose saturation voltage is less their common mode voltage (Vsat < Vcm). In the APEX amplifier line this will almost always be high voltage (+/–Vs > 75V).

For example a PA85 has a common mode voltage of +/–Vs–12 and a saturation voltage of +/–Vs– 5.5 at light loads. For the PA85 the output saturation voltage (5.5V) is less than the common mode voltage (12V from either rail). If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we lower the supply voltage of A1 by about 6.5V, which we can do easily with a zener diode in each supply line of A1. For 200mA output current plus 25mA quiescent current would require at least a 2W, 6.8V zener in each supply rail. The obvious loss with this technique is output voltage swing from the rail, now limited to Vsat of 5.5 Volts plus VRZ drop of 6.8 volts for a total of 12.3V, at light loads.

HIGH POWER w/Vboost(Vsat < Vcm):

This parallel configuration is for amplifiers such as the PA04 or PA05 that are high output current and whose saturation voltage is less than their common mode voltage (Vsat < Vcm.)

For example a PA05 has a common mode voltage of +/–Vs –8 and a saturation voltage of +/–Vs -5.0 at light load. If we try to drive A2 as a unity gain voltage follower directly from A1 we will have a common mode voltage violation. That is, unless we utilize the Vboost function of these power op amps on A2 to run the front end of A2 at a supply voltage which is at least 3 volts above its output voltage supply (Vs). This Vboost supply need only supply quiescent current for the device and can be generated by a switching floating regulator. A less advantageous approach, which would reduce output voltage swing, is to utilize a zener diode in the Vboost supply of A1, similar to the "HIGH VOLTAGE(Vsat < Vcm)" example above.

Ref. AN26

Watch the Follower Phase Shift

- PA85 Power Response Curve = 500KHz@400Vp-p
- Power Design suggests 86KHz for accuracy
- Power Design tells us phase shift is 7°@ 87KHz
- Sin(7°) = 0.122 * 200Vpk = 24.3V

- This voltage appears across the two Rs resistors

The power response graph says you can get to those points, however, you will usually need to increase the drive amplitude and you will probably just start seeing distortion. Another way to put it: these curves demand no loop gain and circuit accuracy is a function of the op amp rather than feedback components on the sloping portion of the power response curve (AC response limits rather than voltage saturation). The amplitude and distortion voltage errors of the follower appear across the two sharing resistors.

Phase shift grows as loop gain decreases. In the primary of the parallel circuit this does no harm locally because the follower input includes the shift. However shift in the follower produces voltage applied across the sum of the two ballast resistors where circulating current becomes a concern.

The Cload sheet of Power Design will calculate closed loop phase shift. The sine of this angle times peak voltage yields the error we are looking for.

Parallel power op amps is <u>not</u> a high speed technique.

Single Supply Parallel Bridge
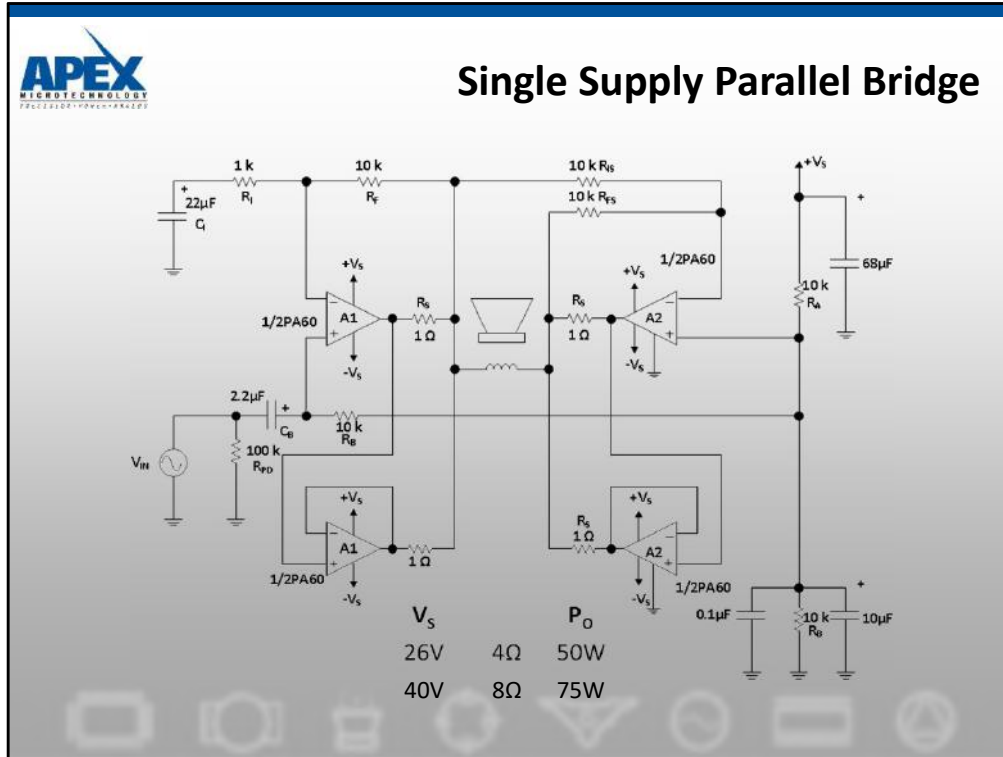
This application utilizes two power op amp circuit tricks—single supply bridge mode to increase output peak-to-peak voltage and parallel power op amps to increase output current.

The PA60 is optimized for single supply operation with its wide input common mode voltage range and low saturation voltage. The parallel combination provides a dual advantage in that we can deliver higher output currents as well as reduce the output saturation voltage since each op amp need only supply one-half the total load current.

AC coupling of Vin provides level shifting of the input signal to swing symmetrically about 1/2Vs. AC coupling through CI ensures the maximum DC offset across the load is only 20mV. RB provides a +input DC bias path for the front end of the primary amplifier half of A1. This is due to the type of output power stage inside the monolithic PA60. A2 is configured as a traditional inverting gain amplifier for single supply bridge mode and uses one half of itself for providing extra current as a follower amplifier in the parallel configuration.

With the PA60 at $5US (1000) this is about 13 cents per watt. PA74 and PA76 offer hermetic packages at higher cost. Just imagine what you could do with PA03s in this circuit. Let's break the KW barrier!

Ref. AN20

Controlling Output Current

- Removes Zload from the Iout equation
- Adds Zload to the Vout equation

- Charge Rate control
  - Batteries, capacitor plate forming power supply active loads, CD welder
- Magnetic field intensity
  - Bearings, deflection, MRI, torque, linear or angular displacement

Controlling current rather than voltage is much more common with power op amps than will small signal op amps. The current control world brings interesting applications plus some new techniques with their own equations and special points to watch.
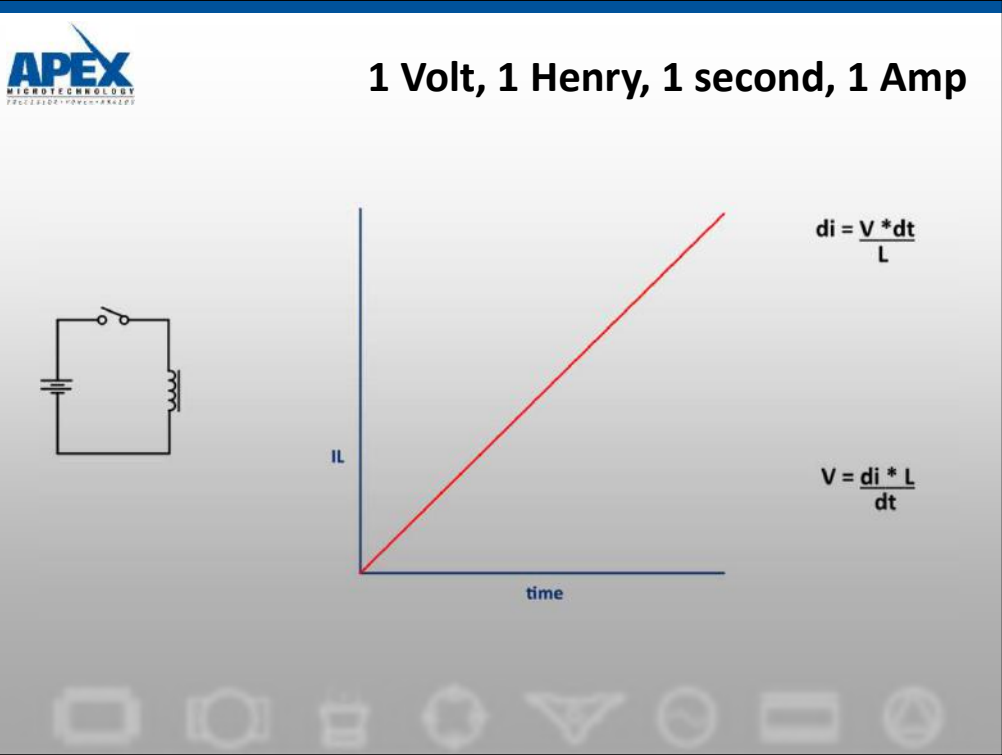
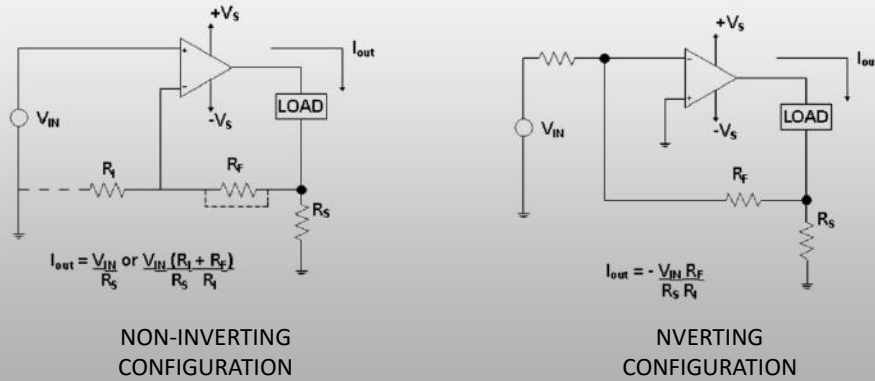OK, so you've seen this before. It is central to current control.

Changing current a lot, in a big inductor, in a hurry, takes lots of volts.

The corollary:

Stopping a big current, in a big inductor, in a hurry, generates lots of volts.

It may require more power than first glance says; opening a current carrying line may release all the stored energy in the form of fire

Voltage-to-Current Conversion

NON-INVERTING CONFIGURATION

$$I_{out} = \frac{V_{IN}}{R_S} \text{ or } \frac{V_{IN}}{R_S} \frac{(R_I + R_F)}{R_I}$$

INVERTING CONFIGURATION

$$I_{out} = -\frac{V_{IN}}{R_S} \frac{R_F}{R_I}$$

Two generic examples of voltage-to-current conversion for a floating load are shown here. The floating load circuit provides the best possible performance of any of the current output circuits with the tradeoff that the load must float.

In the basic non-inverting circuit Ri and Rf don't exist. Load current develops a proportional voltage in Rs which is fed back for comparison to applied input. As long as voltage across Rs is lower than the input voltage, the output voltage increases. In other words the op amp impresses the input voltage on the sense resistor. Adding the resistors allows increasing the transfer function. It is also common to have Rf without Ri providing an RC stabilizing network a reasonable impedance for its AC feedback signal.

The inverting circuit works in the same manner other than polarity but does have the advantage of being able scale the transfer function up or down. This mean it is possible to have less voltage on the sense resistor than the input signal has.

Ref. AN13

18
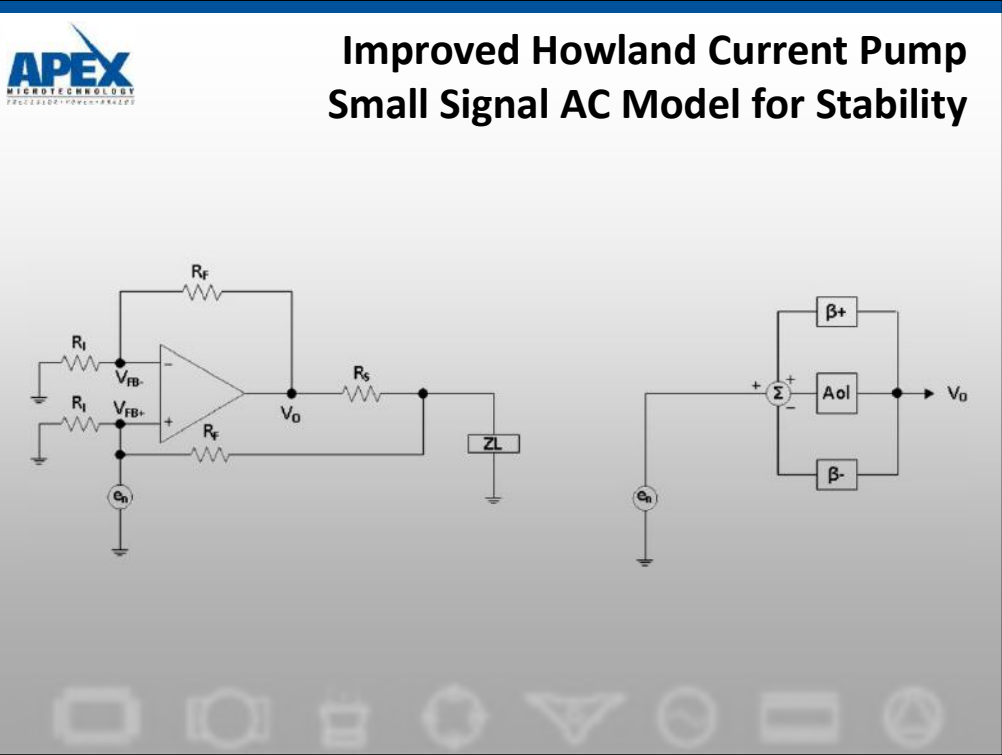
$$\beta+ = \frac{Vfb}{Vo}$$

$$Vo = Aol\,(en + Vo\,\beta+ \; -Vo\beta-$$

$$\beta- = \frac{Ri}{Rf+R}$$

$$Vo \; - Aol\,Vo\,\beta+ \; +Aol\,Vo\,\beta- \; = en\,Aol$$

$$\beta+ = \frac{[ZL||(Rf+Ri)]Ri}{[Rs+ZL||(Rf+R\;)][Rf+Ri]}$$

$$\frac{Vo}{en} = \frac{1}{\beta--\beta+}$$

_____

_____

$$\beta = \; \beta--\beta+ \qquad\qquad \beta = B--\beta+$$

The figure on the left above shows a typical Improved Howland Current Pump circuit. Notice the additional en voltage source on the non-inverting input node of the op amp. For AC small signal stability analysis we do not know where the input signal can be injected. We choose to inject the AC input signal at the +input since this will result in the worst case stability situation. 1/β plots then will be a representation of Vo/en .

The figure on the right above is the equivalent control system block diagram from which we derive the powerful equation for β which will enable us to stabilize the Improved Howland Current Pump with the stability analysis techniques we have previously covered.
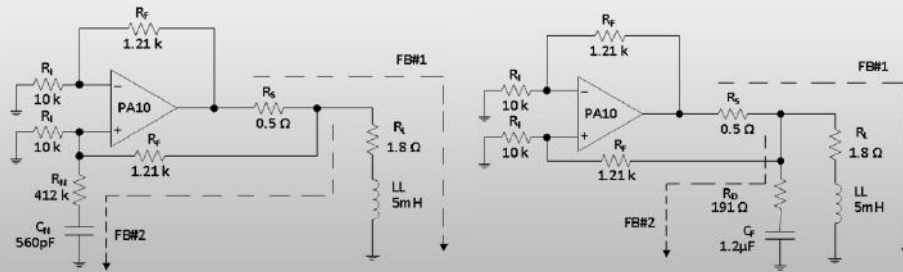
For any engineering problem there is usually more than one solution. This is true when reviewing AC stability compensation for the Improved Howland Current Pump and proposing a solution, or two!

Shown above are two compensation techniques, Compensation 1 and Compensation 2. FB#1 for both compensation techniques will be the same. Similar to V—I circuits for floating loads this β + feedback path which will cause a zero in the net 1/β plot which will result in 40dB per decade rate of closure and instability without additional compensation provided by FB#2.

FB#2 has the function of reducing the voltage fed back to the +input at higher frequencies and thereby forming a pole in the net 1/β plot which guarantees stability and a 20dB per decade rate of closure.

Compensating the Howland Current Pump

10 Steps to Stability

$$I_{out} = V_{IN}/R_S * R_F/R_I$$

$i = const.$
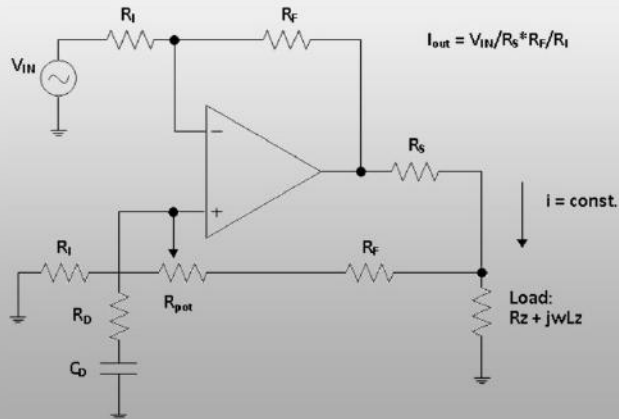
Load:
$R_z + j\omega L_z$

Inductive loads cause stability trouble with current source applications. Because current lags voltage in an inductor, current feedback is delayed and thus decreases the phase margin of the current amplifier. Consequently, ringing or oscillation occurs. This following procedure shows a proper compensation technique for inductive loads.

After choosing Ri, select an appropriate current sense resistor Rs. The voltage available to your load is the power supply voltage minus the voltage drop across Rs. Power dissipation of Rs calculates to Prs = Imax2 * Rs. Continue to calculate the following component values: Finally, adjust Rd and Cd values to standard values and insert a trim pot between the feedback resistor and the input resistor of the positive feedback network:

Rpot = .02*ΔR[%]*(Ri+Rf)[1]

The potentiometer compensates the resistance mismatch of the Rf/Ri network. Trim for maximum output impedance of the current source by observing the minimum output current variation at different load levels and maximum output current.

[1] ΔR[%]: resistor tolerance in percent
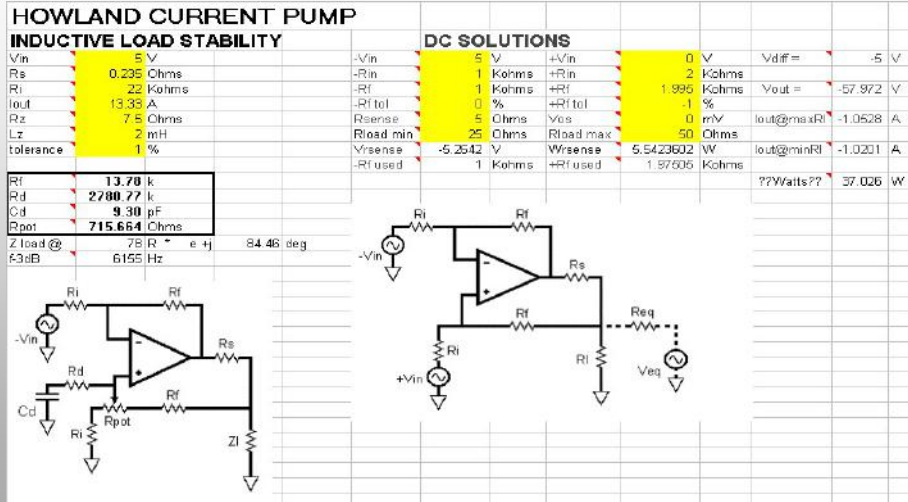
Again, Power Design eases the design burden. Cells to describe the circuit, both for stability analysis and error budget analysis. There are many other pieces of data lying outside this slide if you like to dig around. Application Note 13, Voltage to Current Conversion is the reference.

Voltage-to-Current Conversion

Single Supply, Bridge Mode

+/-Vload LIMITED BY Vcm LIMITS OF A1

This configuration combines two previously covered techniques: single supply bridge configuration and V to I conversion using the improved Howland current pump. A2 is biased at the familiar Vs/2 mid-supply point. Rf and Ri must be ratioed such that during min and max output voltage swings of A1 the common mode input range of A1 is not violated. This imposes a max output voltage swing limit across the load. Iout through the load is given by: Iout=(Vin*Rf)/(Rs*Ri). Rs is selected as large as possible to give as much voltage feedback as possible with acceptable power dissipation. Vin is set to its most positive value. Vcm for A1 (common mode input voltage for A1) is set to comply with data sheet specifications. Usually this will be about Vs-6, which means Vcm must be at least 6.0 volts. Ri is selected to cause about .5 mA to flow through it when Vin is at its most negative voltage. This then dictates the value for Rf which is selected to complete the Vin to Iout equation given above. Vcm should then be rechecked for input common mode compliance at positive and negative swing out of A1. Recall that Vout (A2)=Vs-Vout(A1) for the given circuit. Vout (A1) must be at least Vcm to keep A1 operating in the linear region. Then Vload=(Vs-Vcm)-Vcm. In other words Vload=Vout(A2)-Vout(A1). Therefore, the maximum output peak voltage across the load for this configuration is Vs-(2*Vcm).