PA07R

Radiation Tolerant FET Input Operational Amplifier

RoHS COMPLIANT

FEATURES

- Low Bias Current — FET Input
- Protected Output Stage — Thermal Shutoff
- Excellent Linearity — Class A/B Output
- Wide Supply Range — ±12V to ±50V
- High Output Current — ±5A Peak
- Single Event Effect (SEE) Testing - 62.5 MeV.cm^{2}mg
- Total Ionizing Dose (TID) Testing - 50 krad (Si)

APPLICATIONS

- Fine steering and deformable mirrors
- Laser gimbles
- Reaction wheels
- Laser stabilization and pointing
- Motor drive and piezo drive

DESCRIPTION

The PA07R is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers and/or improper mounting torque will void the product warranty. Please see Application Note 1, “General Operating Considerations.”

APEX RAD TOLERANT OVERVIEW

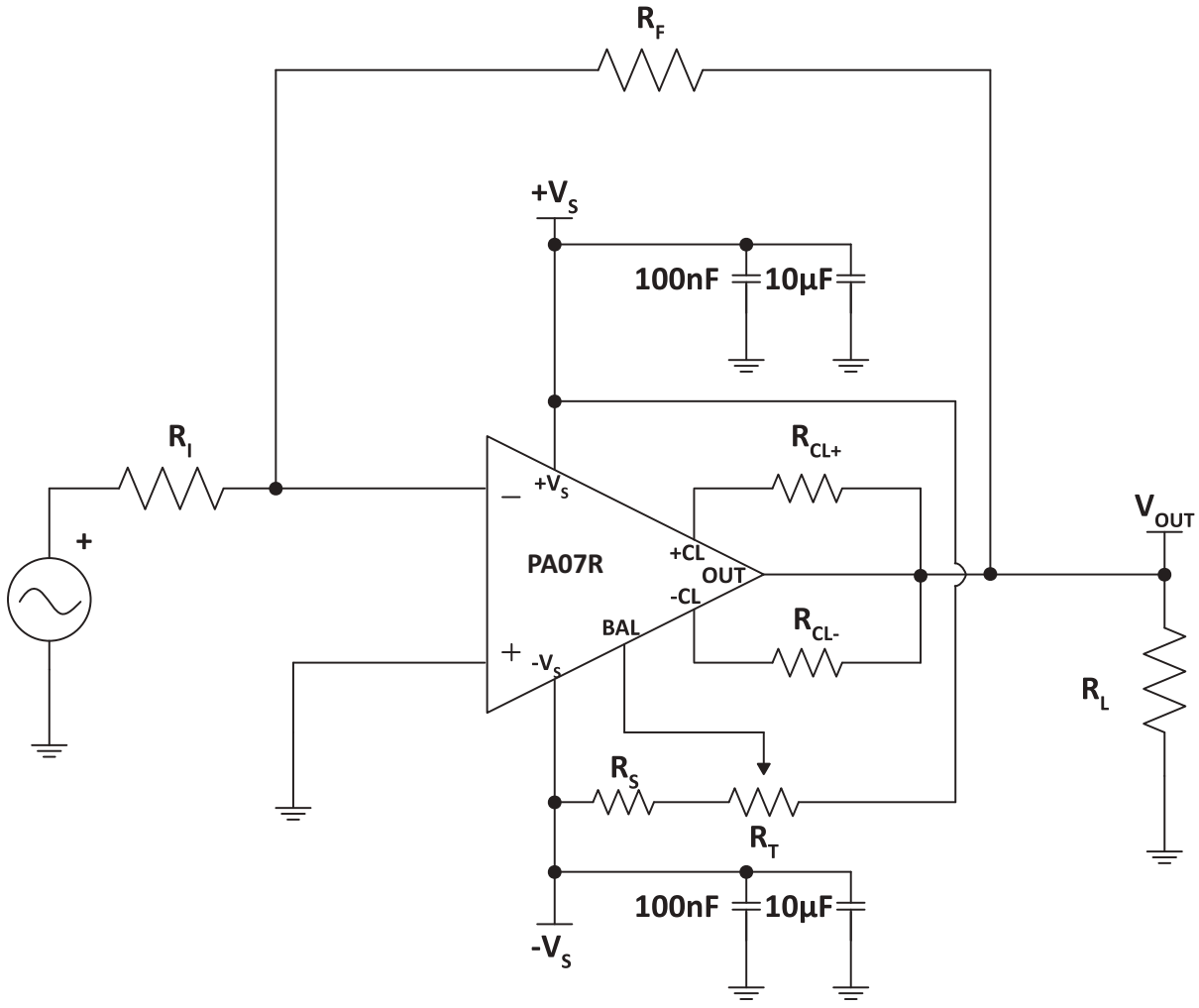
As an Apex radiation tolerant device, PA07R has been tested to “M/883” compliance. Additional testing for radiation tolerance includes:

- Particle Impact Noise Detection (PIND) Testing
- Single Event Effect (SEE) Testing: 62.5 MeV.cm^2/mg, Xenon heavy ion
- Enhanced Low Dose Rate Sensitivity (ELDRS) Testing: Dosage: 50 krad (Si)
- High-Dosage Radiation (HDR) Testing: Dosage: 50 krad (Si)

Apex radiation tolerant devices are considered “Class-H”, or radiation-tolerant. These devices do not satisfy the requirements for “Class-K” or radiation-hardened devices.

TYPICAL CONNECTION

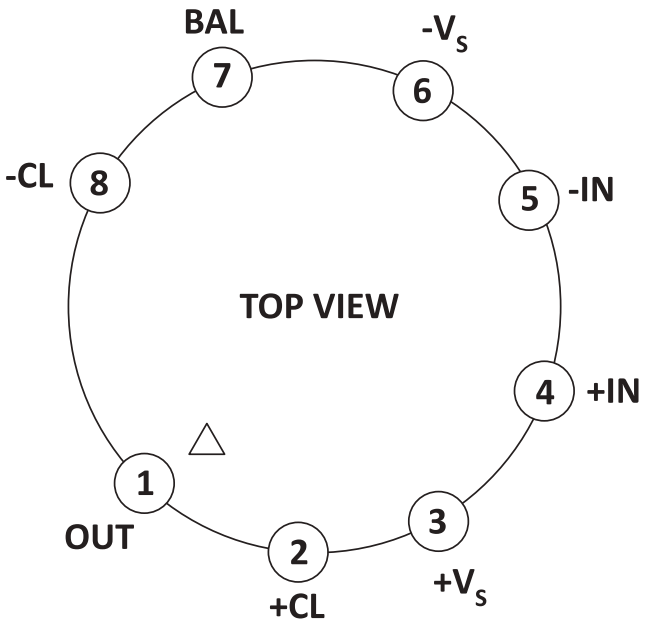
Figure 1: Typical Connection



Note: Input offset voltage trim optional. R_T = 10 kΩ MAX

PINOUT AND DESCRIPTION TABLE

Figure 2: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the current limit resistor. Output current flows into/out of these pins through R_{CL}. The output pin and the load are connected to the other side of R_{CL+}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	BAL	Balance Control pin. Adjusts voltage offset. See applicable section.
8	-CL	Connect to the current limit resistor. Output current flows into/out of these pins through R_{CL}. The output pin and the load are connected to the other side of R_{CL-}.

SPECIFICATIONS

The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		100	V
Output Current, within SOA	I_O		5	A
Power Dissipation, internal [1]	P_D		67	W
Input Voltage, differential	$V_{IN\ (Diff)}$		±50	V
Input Voltage, common mode	V_{cm}		$\pm V_S$	V
Temperature, pin solder, 10s max.			350	°C
Temperature, junction [1]	T_J		200	°C
Temperature Range, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA07			PA07R			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial[3]	T_C = 25°C		0.5	±2		±2.8		mV
Offset Voltage vs. Temperature	Full temp range		10	30		*	*	µV/°C
Offset Voltage vs. Supply	T_C = 25°C		8			*		µV/V
Offset Voltage vs. Power	Full temp range		20			*		µV/W
Bias Current, initial [1,3]	T_C = 25°C		5	50		13		pA
Bias Current vs. Supply	T_C = 25°C		0.01			*		pA/V
Offset Current, initial [1,3]	T_C = 25°C		2.5	50		83		pA
Input Impedance, DC	T_C = 25°C		10^{11}			*		Ω
Input Capacitance	T_C = 25°C		4			*		pF
Common Mode Voltage Range [2]	Full temp range	$\pm V_S$–10			*			V
Common Mode Rejection, DC[3]	Full temp range, V_{CM} = ±20V		120			*		dB

1. Doubles for every 10°C of temperature increase.
2. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
3. Typical values taken from HDR data at 50 krad

GAIN

Parameter	Test Conditions	PA07			PA07R			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop @ 15 Hz[1]	T_C = 25°C, R_L = 15 Ω	89	95			*		dB
Gain Bandwidth Product @ 1 MHz	T_C = 25°C, R_L = 15 Ω		1.3			*		MHz
Power Bandwidth	T_C = 25°C, R_L = 15 Ω		18			*		kHz
Phase Margin	Full temp range, R_L = 15 Ω		70			*		°

1. Typical values taken from HDR data at 50 krad

OUTPUT

Parameter	Test Conditions	PA07			PA07R			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	Full temp range, I_O = 5A	$\pm V_S$–5			*			V
Voltage Swing [1,2]	Full temp range, I_O = 2A	$\pm V_S$–5				$\pm V_S$–4		V
Voltage Swing [1]	Full temp range, I_O = 90mA	$\pm V_S$–5			*			V
Current, peak	T_C = 25°C	5			*			A
Settling Time to 0.1%	T_C = 25°C, 2V step		1.5			*		µs
Slew Rate	T_C = 25°C		5			*		V/µs
Capacitive Load, unity gain	Full temp range,			1			*	nF
Capacitive Load, gain>4	Full temp range,			SOA			*	

1. $+V_S$ and $–V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $–V_S$.
2. Typical values taken from HDR data at 50 krad

POWER SUPPLY

Parameter	Test Conditions	PA07			PA07R			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±12	±35	±50	*	*	*	V
Current, quiescent[1]	T_C = 25°C		18	30		16.5		mA

1. Typical values taken from HDR data at 50 krad

THERMAL

Parameter	Test Conditions	PA07			PA07R			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	F>60 Hz		1.9	2.1		*	*	°C/W
Resistance, DC, junction to case	F<60 Hz		2.4	2.6		*	*	°C/W
Resistance, junction to air			30			*		°C/W
Temperature Range, case	Meets full range specs	-25	25	+85	*	*	*	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: *The specification of PA07R is identical to the specification for PA07 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 3: Power Derating

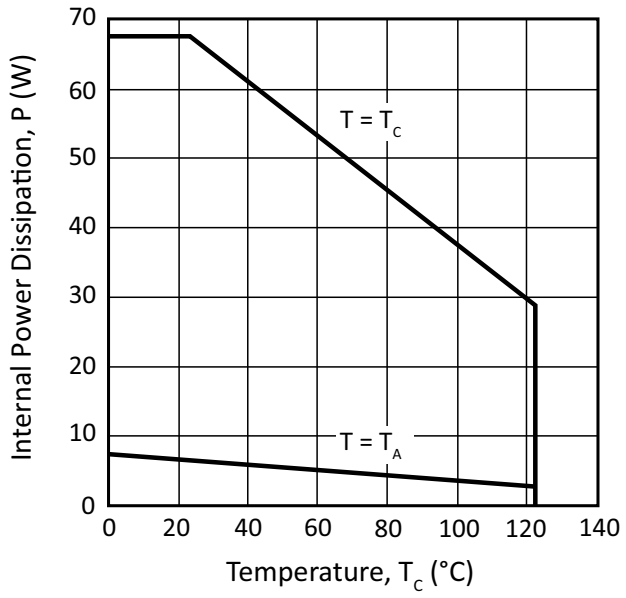


Figure 4: Bias Current

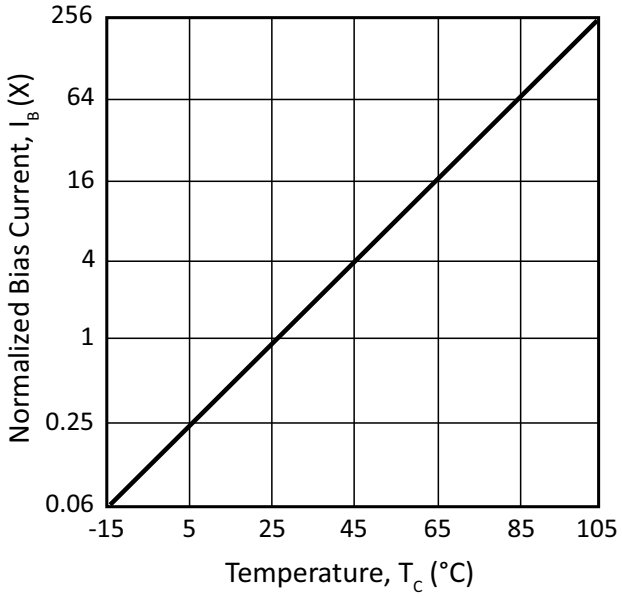


Figure 5: Small Signal Response

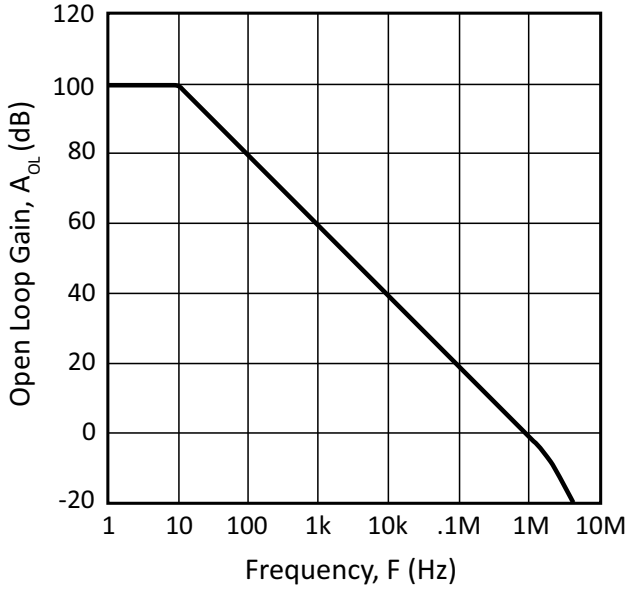


Figure 6: Phase Response

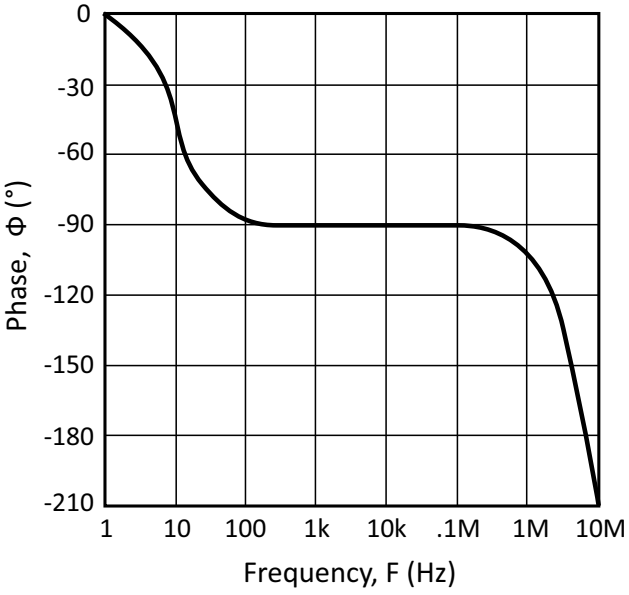


Figure 7: Current Limit

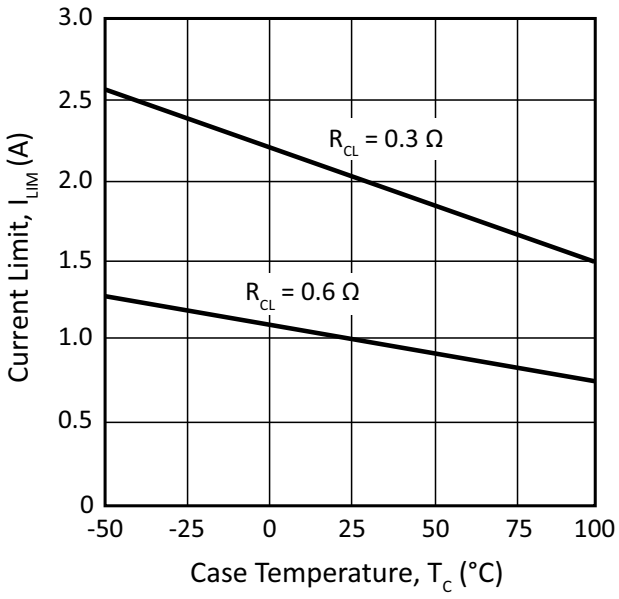


Figure 8: Power Response

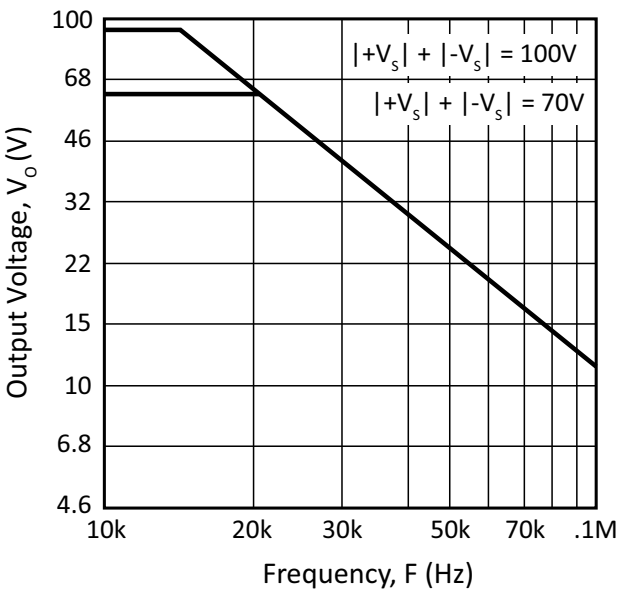


Figure 9: Common Mode Rejection

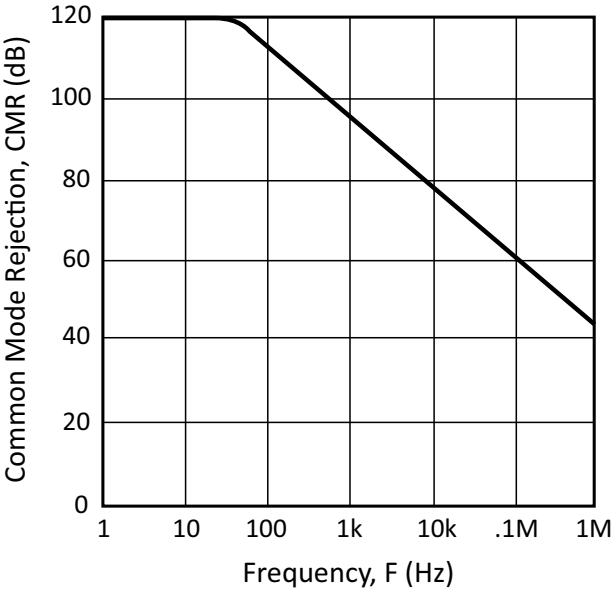


Figure 10: Pulse Response

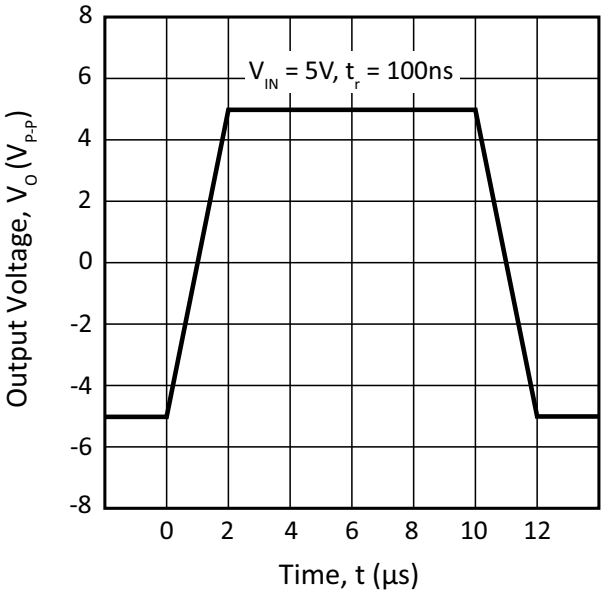


Figure 11: Input Noise

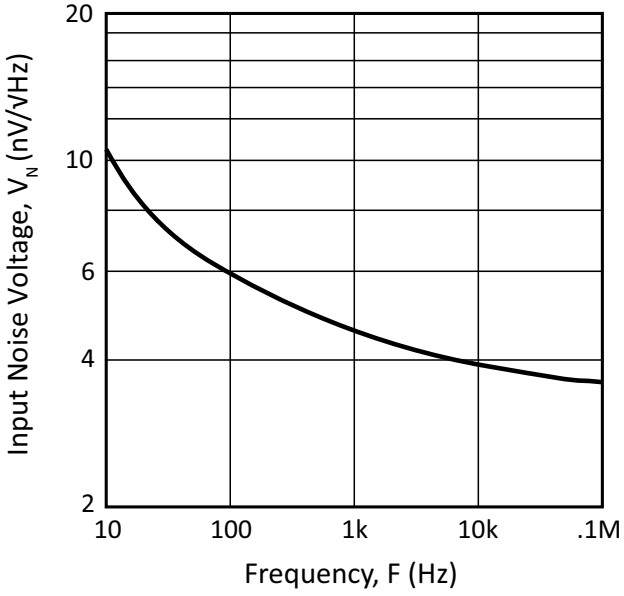


Figure 12: Harmonic Distortion

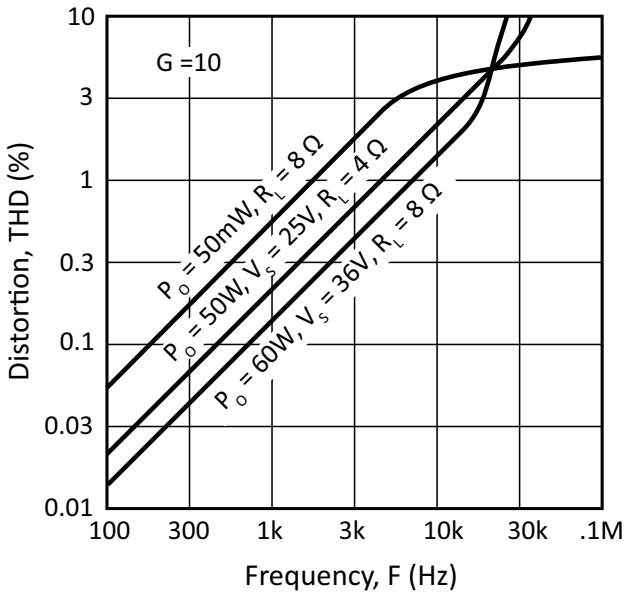


Figure 13: Quiescent Current

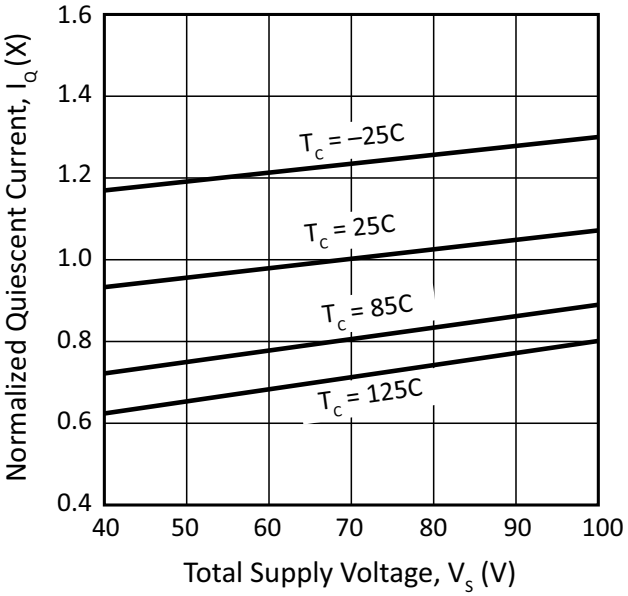
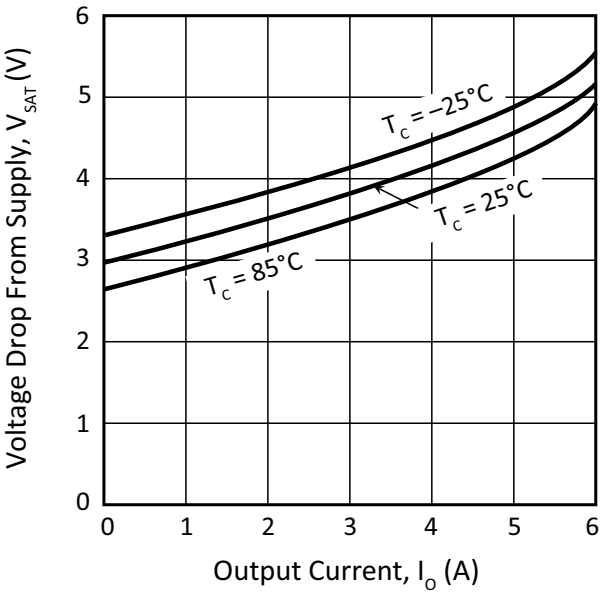


Figure 14: Output Voltage Swing



SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

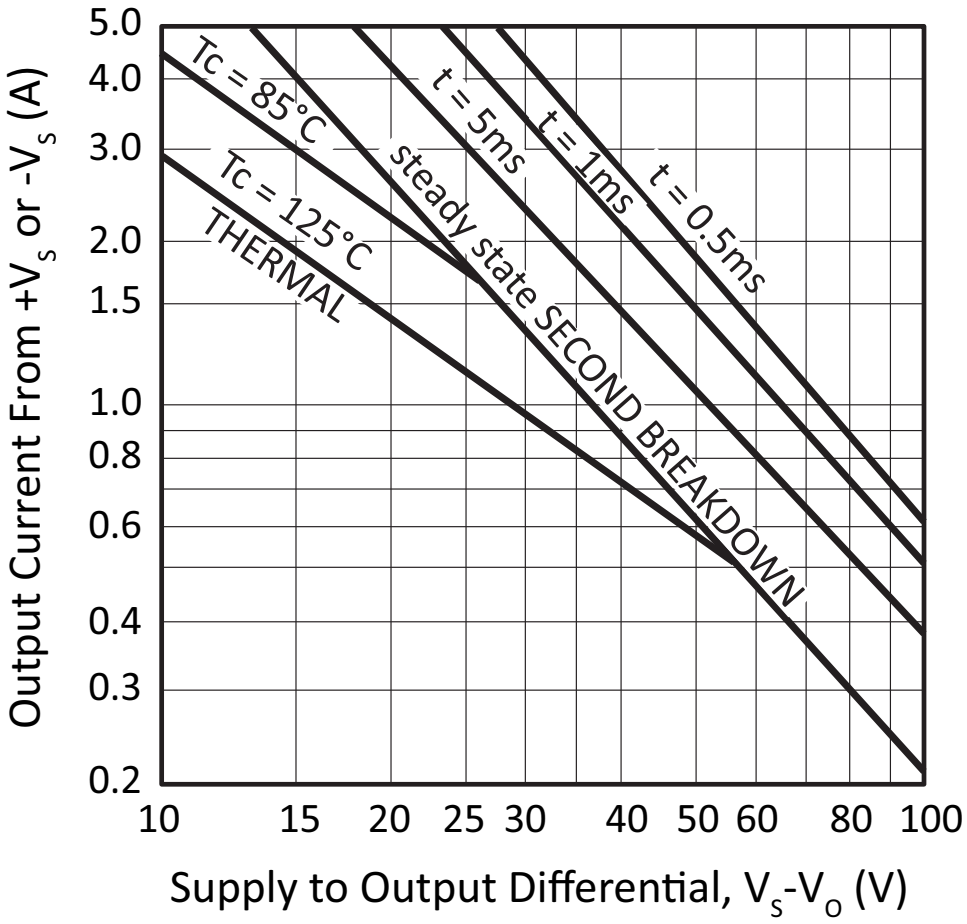
1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the SOA graph.
   Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.
   A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges. Please refer to Application Notes, AN01 and AN22 for detailed information regarding SOA considerations.
2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	Short to $\pm V_S$ C, L, or EMF Load	Short to Common
50V	0.21A	0.61A
40V	0.3A	0.87A
30V	0.46A	1.4A
20V	0.87A	2.5A
15V	1.4A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

Figure 15: SOA



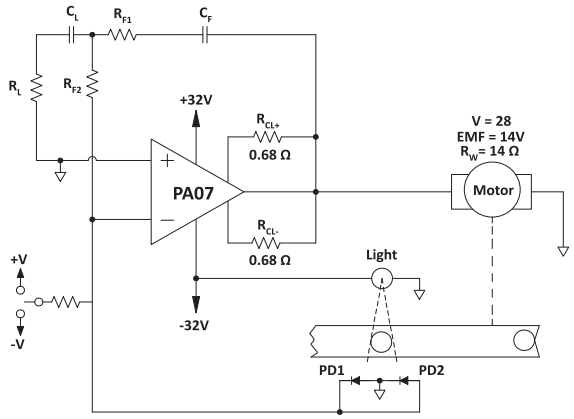
GENERAL

Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C_L and R_L optimize system response by reducing overshoot. The very low bias current of the PA07R augments performance of the integrator circuit.

Figure 16: Typical Application



Note: Negates optoelectronic instabilities; Lead network minimizes overshoot; Sequential Position Control

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for R_{CL} is 0.12 Ω; however, for optimum reliability it should be set as high as possible. Refer to Application Note 1 and 9 for current limit adjust details.

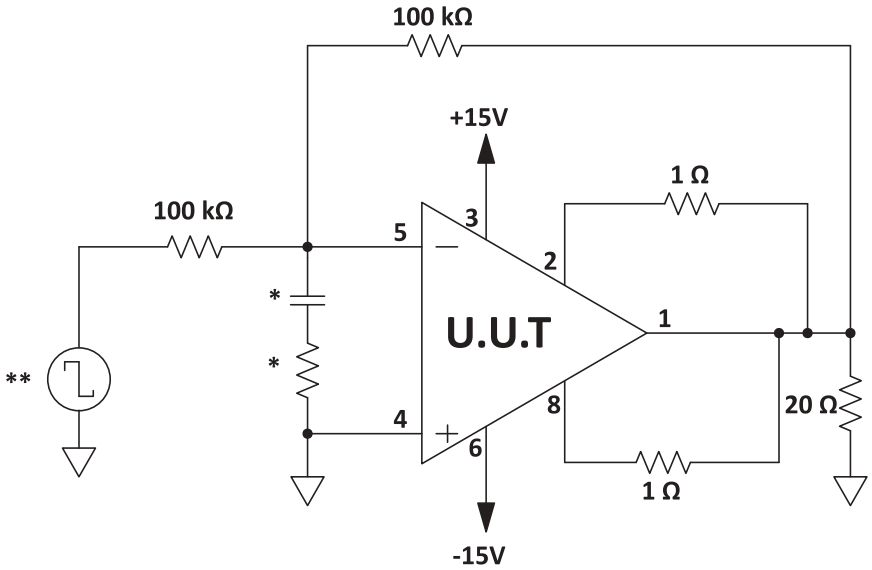
$$R_{CL}(\Omega) = \frac{0.65V}{I_{LIM}(A)}$$

TABLE 4 GROUP A INSPECTION

SG	Parameter	Symbol	Temp.	Power	Test Conditions	Min	Max	Units
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		4.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		46	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		6.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±50V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input Bias Current, –IN	$-I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		30	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		7.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±15.3V	R_L = 2.07 Ω	10.3		V
4	Output Voltage, I_O = 90mA	V_O	25°C	±50V	R_L = 500 Ω	45		V
4	Output Voltage, I_O = 2A	V_O	25°C	±29V	R_L = 12 Ω	24		V
4	Current Limits	I_{CL}	25°C	±19V	R_L = 12 Ω, R_{CL}= 1 Ω	0.54	0.86	A
4	Stability/Noise	E_N	25°C	±35V	R_L =100 Ω, A_V =1, C_L =1nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500 Ω	2.5	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500 Ω, F = 15 Hz	89		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L=500 Ω, F=DC, V_{CM} = ±24.5V	80		dB

SG	Parameter	Symbol	Temp.	Power	Test Conditions	Min	Max	Units
6	Output Voltage, I_O = 5A	V_O	–55°C	±15.3V	R_L = 2.07 Ω	10.3		V
6	Output Voltage, I_O = 90mA	V_O	–55°C	±50V	R_L = 500 Ω	45		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±29V	R_L = 12 Ω	24		V
6	Stability/Noise	E_N	–55°C	±35V	R_L =100 Ω, A_V =1, C_L =1nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500 Ω	2.5	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500 Ω, F = 15 Hz	89		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L=500 Ω, F=DC, V_{CM} = ±24.5V	80		dB
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07 Ω	6.3		V
5	Output Voltage, I_O = 90mA	V_O	125°C	±50V	R_L = 500 Ω	45		V
5	Output Voltage, I_O = 2A	V_O	125°C	±29V	R_L = 12 Ω	24		V
5	Stability/Noise	E_N	125°C	±35V	R_L =100 Ω, A_V =1, C_L =1nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500 Ω	1.25	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500 Ω, F = 15 Hz	89		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L=500 Ω, F=DC, V_{CM} = ±24.5V	80		dB

BURN IN CIRCUIT



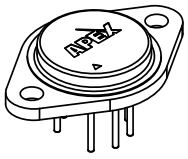
*These components are used to stabilize device due to poor high frequency characteristics of burn in board.

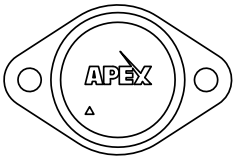
** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PACKAGE OPTIONS

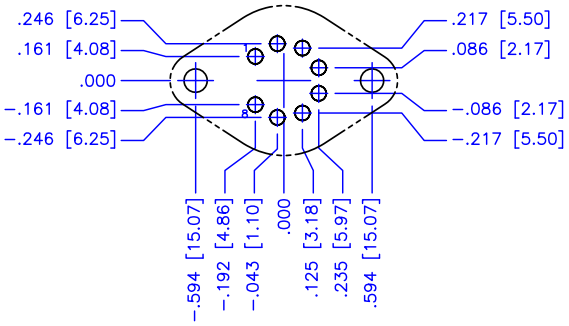
Part Number	Apex Package Style	Description
PA07	CE	8-pin TO-3
PA07R	CE	8-pin TO-3

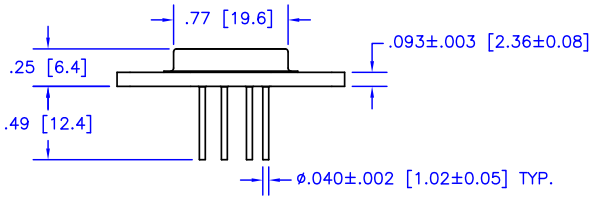
PACKAGE STYLE CE

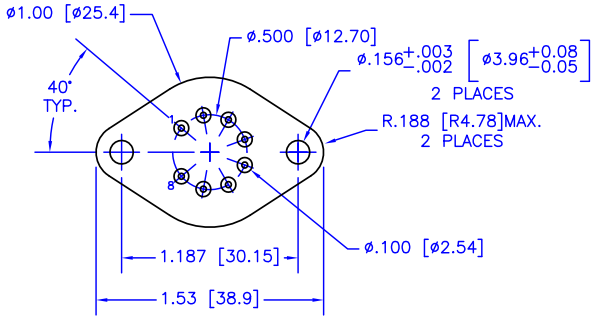




Ordinate dimensions for CAD layout







NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel−plated Alloy 52.
6. Header material: Nickel−plated cold−rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

For all Apex Microtechnology product questions and inquiries, call toll free 800-546-2739 in North America. For inquiries via email, please contact apex.support@apexanalog.com. International customers can also request support by contacting their local Apex Microtechnology Sales Representative. To find the one nearest to you, go to www.apexanalog.com