Power Systems Design: Empowering Global Innovation

Boosting output in high-voltage op-amps with a current buffer

Author: Joe Kyriakakis, Apex Microtechnology
Date: 02/18/2014

Categories: Current, Design Tools, High Voltage, MOSFETs & Power MOSFETs, Op Amps & References

Creating a composite op-amp comes with its own set of design challenges

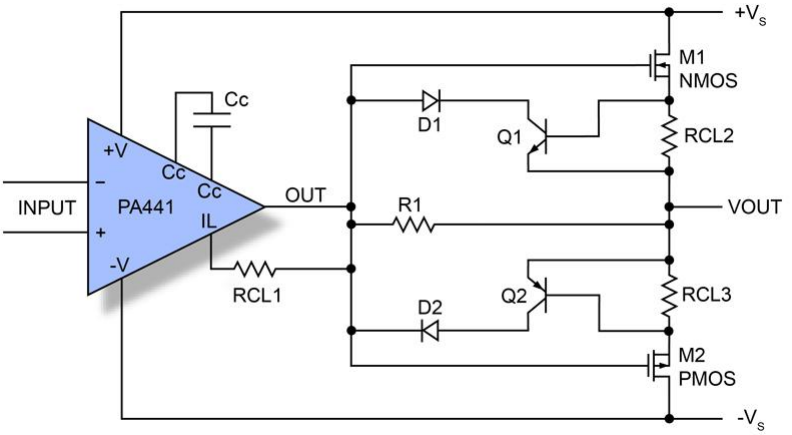
Delivering more than 200mA of output current can be a serious challenge for many high-voltage operational amplifiers. But for high voltage applications requiring as much as 1A of current, it is possible to meet this spec by pairing a current buffer with the op amp. What the current buffer brings to this arrangement is approximate unity voltage gain when it's placed between the output of the high voltage op amp and the load. This means the current buffer is included in the feedback loop of the op amp to create a composite op amp.

But creating such a composite op amp does come with its own set of design challenges. Starting with the current buffer's output stage bias circuit. A Class B output stage may be adequate for some applications, but it has characteristic crossover distortion as the low side device output current transitions to the high side device. The preferred scenario is to use a Class AB output stage as the crossover distortion is much lower and the feedback loop remains closed during the transition. But setting the quiescent current of the Class AB output stage is difficult because of output device variations and sensitivities.

The current buffer design approach explored here makes it possible to avoid many of the design difficulties related to output stage biasing by incorporating a depletion mode MOSFET as the high side driver. This circuit topology exploits the MOSFET's ability to provide the bias current by using it as a current source. The depletion mode MOSFET then serves as both the bias current generator and the high side driver.

Building A Better Buffer

The Class B circuit shown in Figure 1 illustrates one common method of implementing a current buffer. Resistor R1 provides a current path to the load from the high voltage op amp (PA441) and is set to limit the maximum gate voltage of the MOSFETs M1 and M2 to 10V. The resistor RCL1 is used to set the current limit value of the PA441 so that the current in R1 creates a voltage drop of 10V. The op amp current limit value should be set as low as possible to minimize the amount of power dissipation dumped on the op amp. Resistors RCL2 and RCL3 are tasked with providing a level of protection for the output devices by serving to current limit the output MOSFETs.

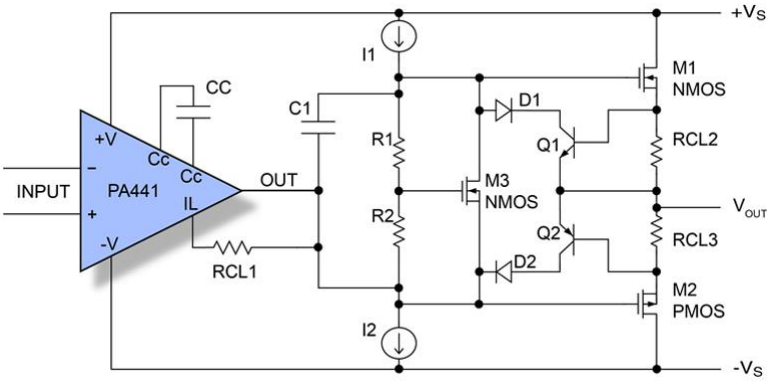


Click image to enlarge

Figure 1: Class B circuit showing one common method of implementing a current buffer

The output current flows through RCL2 and RCL3 creating a voltage across the base to the emitter of Q1 and Q2. Once this voltage reaches approximately 0.7V, the transistors Q1 and Q2 begin conducting current to the load thus clamping the gate drive voltage at M1 and M2 as the PA441 enters current limit mode.

The conventional circuit topology of a Class AB current buffer output stage is illustrated in Figure 2. This is a simplified schematic diagram using a VGS multiplier composed of M3, R1 and R2 to set the required voltage at the gates of M1 and M2. This provides the desired quiescent current through the output devices M1 and M2. Constant current sources I1 and I2 supply the required current to the VGS multiplier. The transistors Q1 and Q2 are used for current limiting as described in the previous Class B stage example.



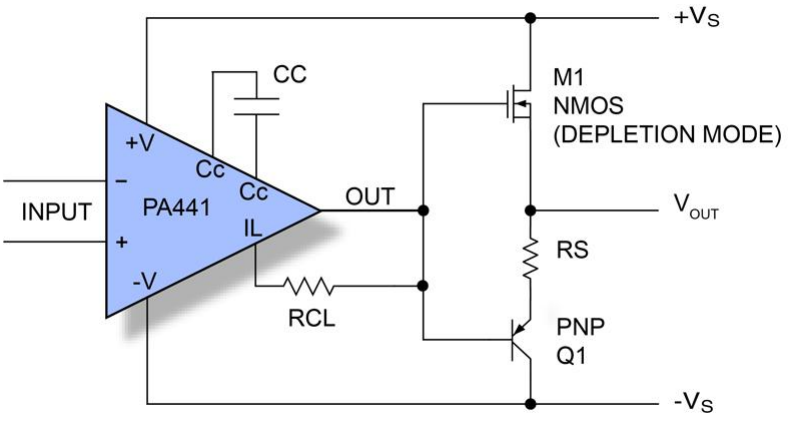
Click image to enlarge

Figure 2: Conventional circuit topology of a Class AB current buffer output stage

This Class AB design approach is much more complex and more problematic than the Class B stage design. First, additional components are required in order to implement the current sources I1 and I2, and the voltage swing will be less than the voltage swing of the PA441 because of the drive requirements of the output MOSFETs. Setting the quiescent current through M1 and M2 is difficult because of the high sensitivity between VGS and ID. The VGS multiplier, consisting of M3, R1 and R2, must be individually adjusted for every unit. To prevent thermal runaway, the circuit relies on device matching and tight thermal coupling between M1, M2 and M3. Taking these factors into account, along with temperature instability and sensitivity in setting the quiescent current, the actual implementation of this circuit topology is much more challenging than that of the Class B buffer version.

There Is An Alternative

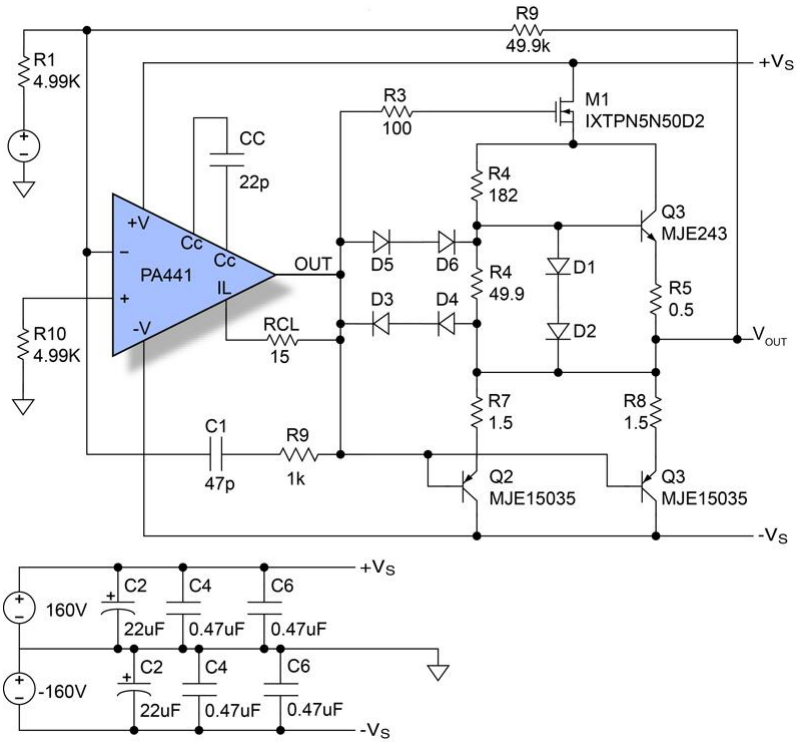
A simplified conceptual circuit diagram of an alternative Class AB topology is shown in Figure 3. This circuit functions in a self-biasing mode and does not require the current sources and VGS multiplier of the conventional Class AB stage. To demonstrate the mechanism for establishing the flow of quiescent current, assume the output voltage is at zero volts. The base of Q1 must be approximately -0.7V. The gate of M1 is also at -0.7V, forcing the MOSFET to conduct. The resistor RS is selected to adjust the quiescent current to the desired value.



Click image to enlarge

Figure 3: A simplified conceptual circuit diagram of an alternative Class AB topology

The actual prototype of this circuit schematic is shown in Figure 4. The depletion mode MOSFET M1 is biased to provide the quiescent current for the output stage. Resistors R4 and R5 are selected to establish the operating current of M1. The bipolar transistor Q1 acts as a Vbe multiplier to maintain the desired VGS for M1 as the demand for load current increases. So Q1 essentially conducts the output current sourced by M1 by bypassing R4 and R5. The bipolar transistors Q2 and Q3 are biased by the quiescent current and provide the load current during the negative half cycle.



Click image to enlarge

Figure 4: A prototype of the circuit schematic

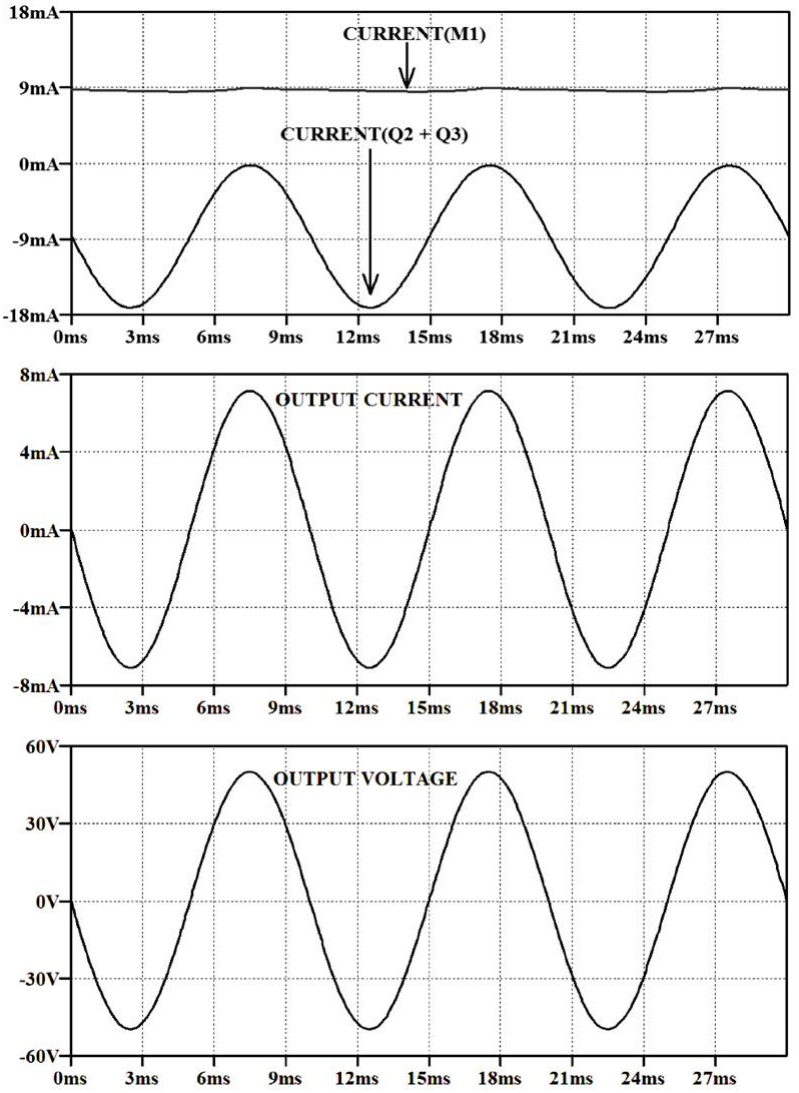
Two PNP transistors are necessary to accommodate the required power dissipation. The maximum rated power dissipation of each PNP transistor is 50W. The current limit function is implemented through the addition of diodes D1 through D6. The diodes used in the prototype are 1N4148, but any equivalent small signal switching diode such as 1N914 is suitable. As the output current approaches approximately 1.2A, the voltage across R6 in series with the Vbe of Q1, forces Q1 to limit the output current. Since the diodes D1 and D2 are conducting, a constant current through Q1 is established. The maximum output current delivered by the PA441 is set to approximately 40mA by Rcl.

The diodes D5 and D6 clamp the output of the PA441 to limit the VGS of M1 and still provide sufficient gate drive voltage to support the load current. When the current limit function is engaged, the output current of the

PA441 flows through D1, D2, D5 and D6. The current limit for the negative half cycle functions by forcing output current from the PA441 through diodes D3 and D4, which establishes a constant current of approximately 1.2A through Q2 and Q3.

This alternative topology does offer several advantages including a high output voltage swing resulting from a limited voltage drop as compared to the typical enhancement mode Class AB output stage; the simplicity of setting quiescent current; and a big plus, a reduced component count.

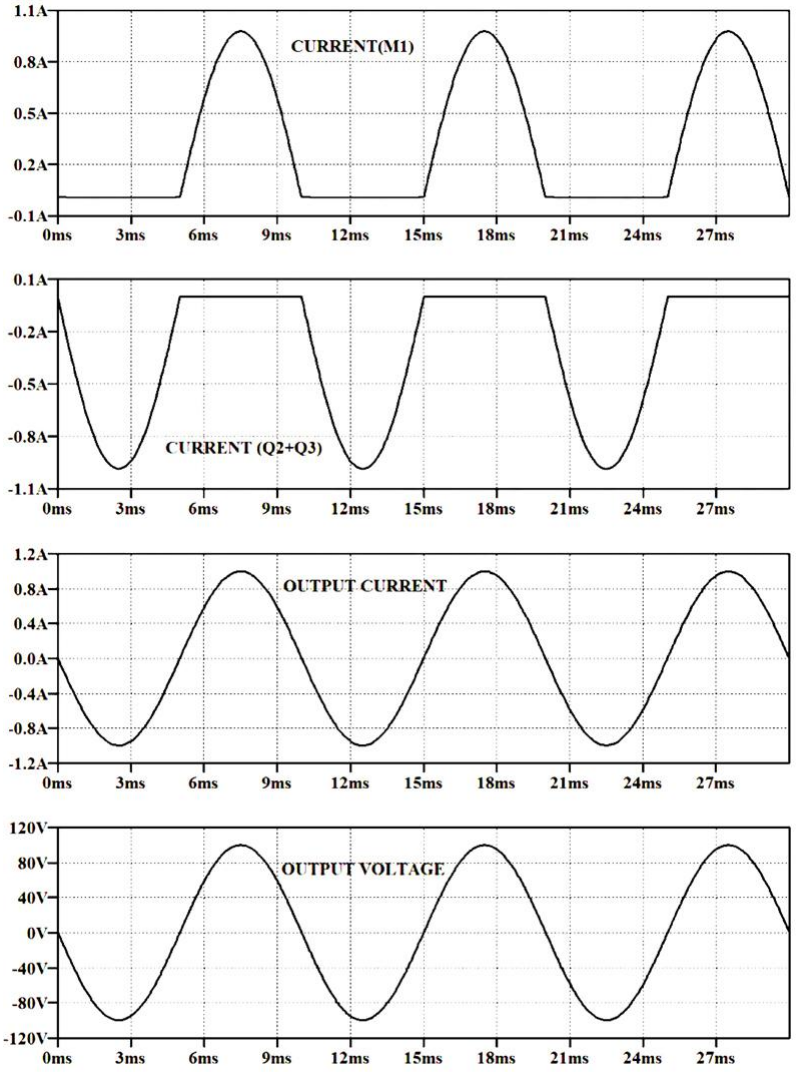
The simulation plots shown in Figure 5 demonstrate the output stage behavior in Class A mode operating under light load conditions. These plots indicate the output voltage is 100V p-p across a load resistor of approximately 7KΩ with quiescent current of approximately 9mA. Since the current through the transistors M1, Q2 and Q3 is always greater than zero for the entire cycle, the output stage is operating in Class A mode.



Click image to enlarge

Figure 5: Output stage behavior in Class A mode operating under light load conditions

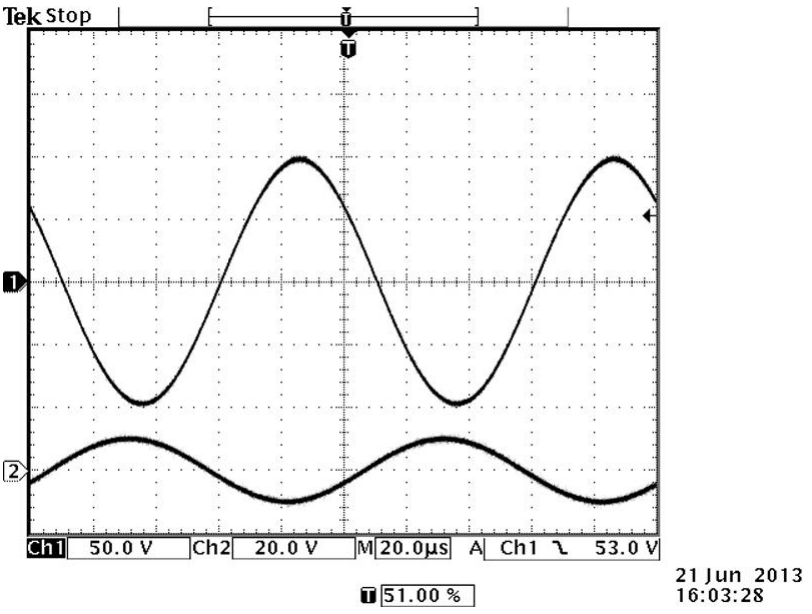
In comparison, the simulation plots of Figure 6 Illustrate the output stage behavior in Class AB mode circuit operation under full load conditions. In this scenario, the power supply volt¬age is ±160V and the output voltage is 200V p-p across a load resistor of 100Ω.



Click image to enlarge

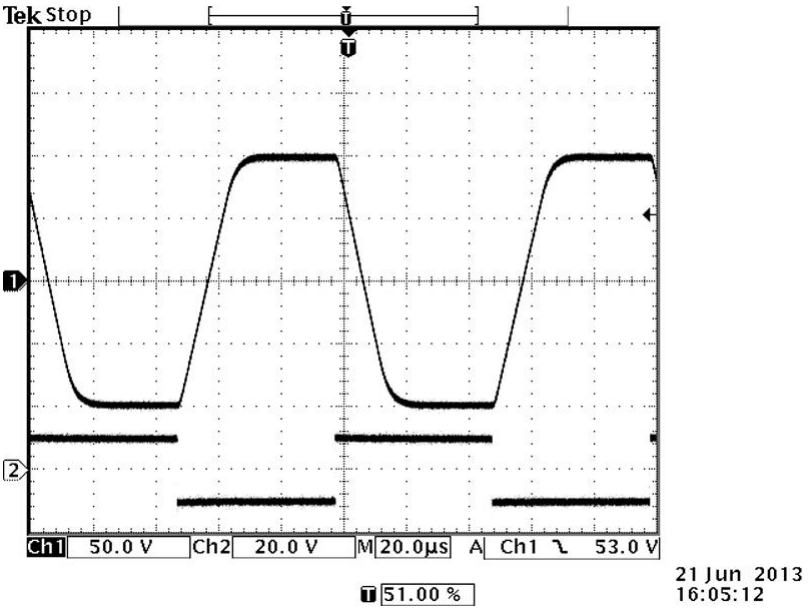
Figure 6: Output stage behavior in Class AB mode circuit operation under full load conditions

Figures 7, 8, 9 and 10 are oscilloscope screen shots taken during bench testing showing the actual circuit behavior. Power supply voltage is ±160V, and signal frequency is 10KHz, with the amplifier configured for an inverting gain of 10. The actual circuit configuration is shown in Figure 4. Channel one is the output voltage and channel two is the input voltage.



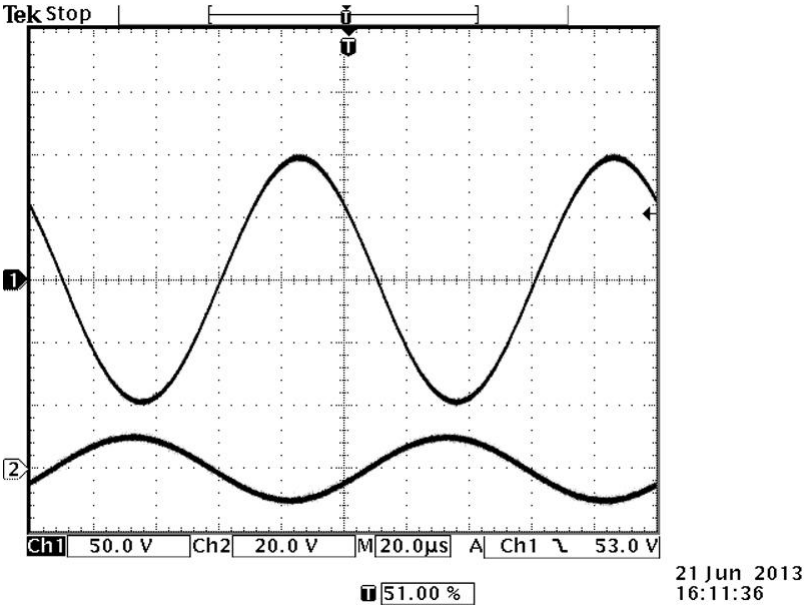
Click image to enlarge

Figure 7: Oscilloscope screen shots taken during bench testing (Part 1)



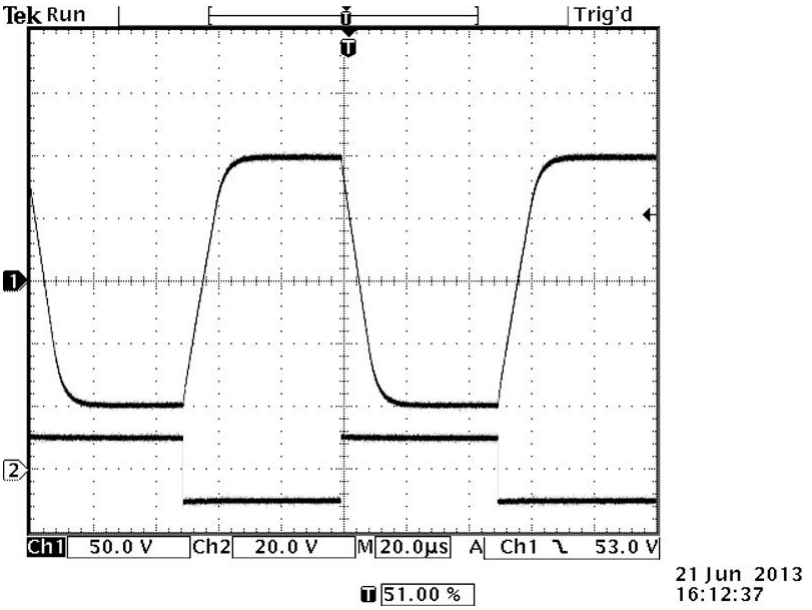
Click image to enlarge)

Figure 7: Oscilloscope screen shots taken during bench testing (Part 2)



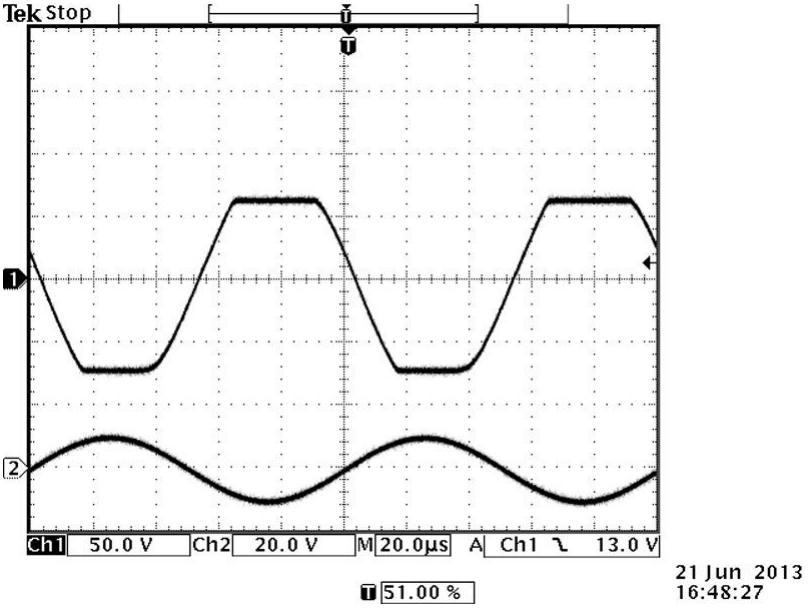
Click image to enlarge

Figure 8: Oscilloscope screen shots taken during bench testing (Part 1)



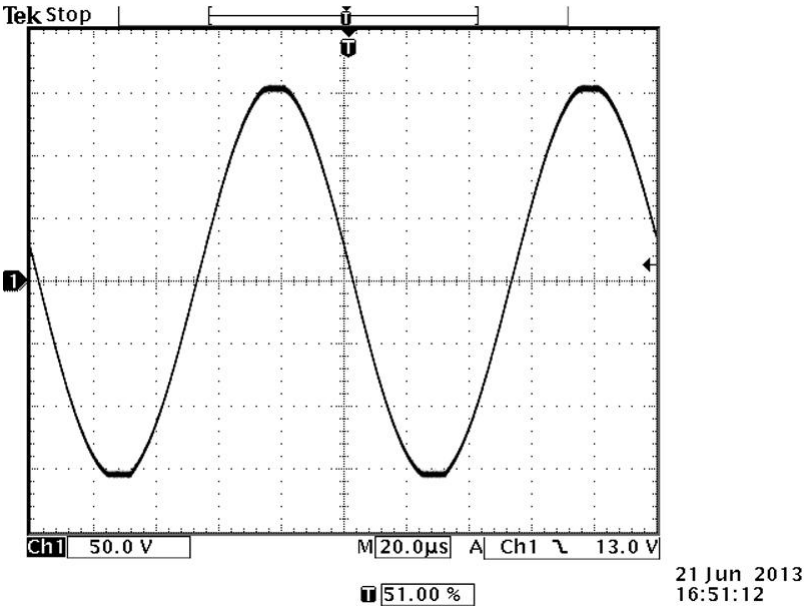
Click image to enlarge

Figure 8: Oscilloscope screen shots taken during bench testing (Part 2)



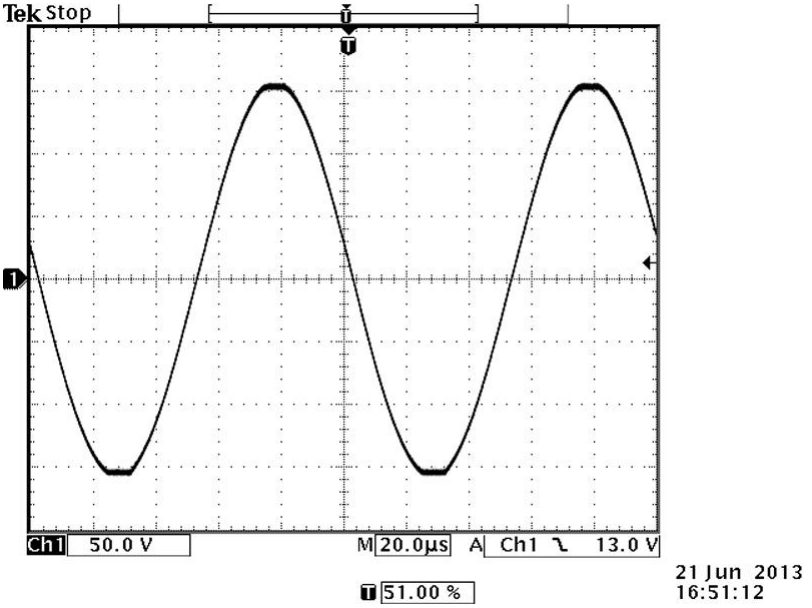
Click image to enlarge

Figure 9: Oscilloscope screen shots taken during bench testing (Part 1)



Click image to enlarge

Figure 9: Oscilloscope screen shots taken during bench testing (Part 2)



Click image to enlarge

Figure 10: Oscilloscope screen shots taken during bench testing

In summary, it is possible to take a high voltage op amp and give it the opportunity to deliver equally impressive output current. Hopefully this article has demonstrated it is possible to meet this challenge with relative ease by pairing the op amp with a current buffer. Now the choice of buffer circuitry is up to you.

Apex Microtechnology