Cycle-by-Cycle Current Limiting Eases Design of Motor Drives

The integration of this protection feature within brushless dc motor-driver ICs protects the motor driver against high inrush currents without adding to pc-board space requirements or driver complexity.

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Brushless dc motors have the advantages of high reliability and smaller size, but the absence of brushes can pose challenges. One challenge is the requirement for electronic commutation and control, but the plummeting cost of processing power reduces the financial impact of this increased complexity. An additional challenge is the elimination of brush resistance, which causes inrush current to be substantially higher than average-run current.

For example, a 1-A continuous motor current might require a drive amplifier to deliver well over 10-A peak current to accommodate the initial inrush startup current. Low-inertia brushless motors can have a peak-to-average current ratio above 30, which leaves a designer with the choice of either selecting a driver that can safely handle the large inrush current or installing adequate current limiting.

The high current solution requires a look at the rise in back electromagnetic force (EMF), which corresponds to the motor velocity and the current (Fig. 1). Clearly, an

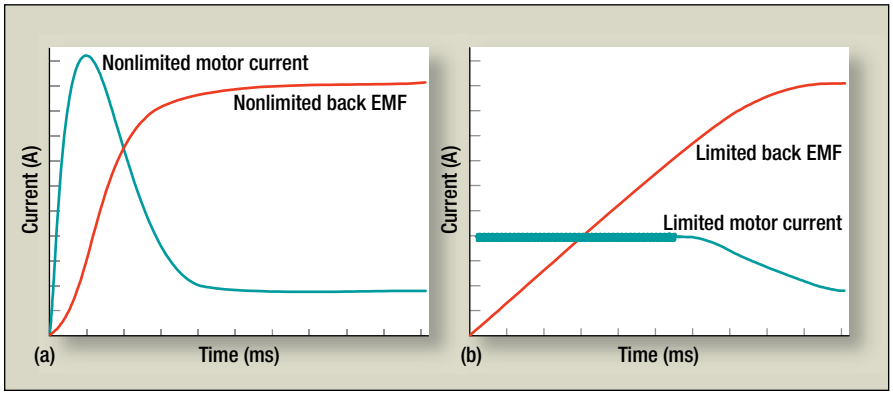

Fig. 1. *Brushless motor current startup behavior without cycle-by-cycle current limiting (a) and with cycle-by-cycle current limiting (b).*

unlimited current motor accelerates faster and can be a benefit in some applications. But in many cases, acceleration is not the critical measure of performance, so the drive circuit size can be cut by limiting the current.

Rotor Dynamics

Startup is a stressful time for a brushless motor-drive circuit. When at rest, the motor generates no back EMF (V_{BEMF}), thus the drive voltage and passive motor characteristics are the only contributors to motor current. When the motor spins up, it generates back EMF, easing the current demands on the drive circuit. The red line in Fig. 1 depicts V_{BEMF} behavior.

Applying voltage to the motor causes the rotor to begin turning, generating V_{BEMF} as governed by this calculation:

$$V_{BEMF} = K_B \times \text{speed}, \quad \text{(Eq. 1)}$$

where K_B equals the motor voltage constant (volts/1000 rpm) and speed equals revolutions per minute (expressed in thousands).

Therefore, motor current is:

$$I = \left[\frac{V - V_{BEMF}}{R}\right]\left[1 - e^{\frac{t_R}{L}}\right], \quad \text{(Eq. 2)}$$

where I equals the motor current in amperes, V equals the applied drive voltage in volts, t equals the time in seconds, R equals the stator resistance (winding pair) in ohms and L equals the stator inductance (winding pair) in henries.

These equations apply to both brush and brushless motors, but the absence of brush resistance makes the exponential R/L term in Eq. 2 a more-significant factor for brushless motors. Although the inrush current may last only for a brief moment, a drive stage without current limiting must use an output stage capable of safely handling the large inrush current. Whether the output drive stage is an IC or a discrete collection of MOSFETs, a high current output generally implies an increase in package size, pc-board layout area and overall cost.

Current-Limit Functionality

As with many motor-drive discussions, the concept of current limiting in the context of a pulse-width-modulated (PWM) circuit is straightforward. Simply measure the current in each motor phase or each drive leg, and turn off the drive transistors when the current reaches some programmable threshold. Then let the current decay in the motor for the rest of the PWM cycle, begin a new PWM cycle and repeat the process. The PWM voltage and current waveforms are similar to those in Fig. 2.

A look at Fig. 2 reveals the cycle-by-cycle current-limit behavior. During the first PWM pulse, no current limiting occurs, because the pulse ends before the rising current

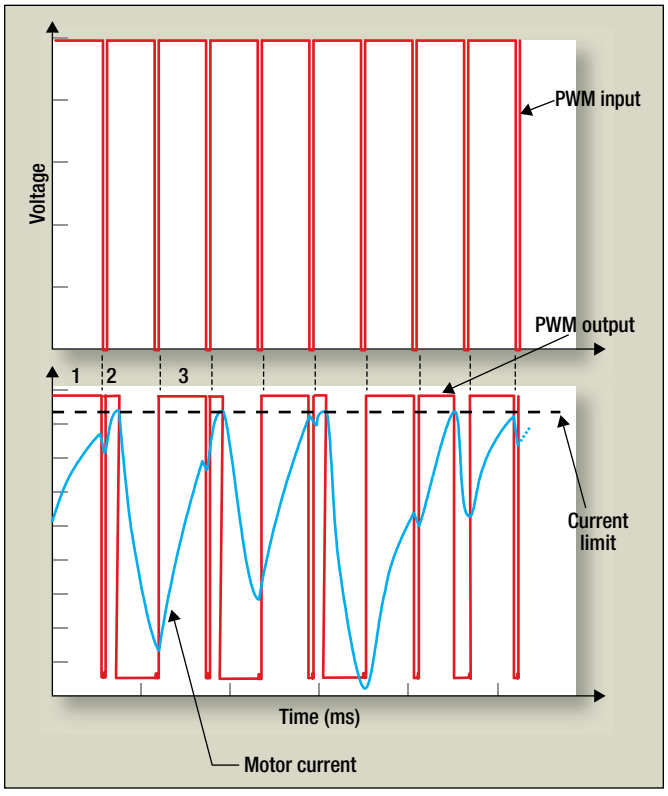

Fig. 2. *Cycle-by-cycle current limiting with PWM control varies as the motor spins.*

reaches the current-limit threshold. At the end of the first pulse, there is a short decay before the second PWM pulse begins and the current resumes its rise.

During the second PWM pulse, the current reaches the limiting value before the PWM input pulse ends. The PWM output pulse is shut off early in its cycle. Then the motor current decays until the third pulse is applied, which once again causes the current to rise.

This behavior continues until the motor rotation begins to generate sufficient back EMF for the current to fall below the current-limit threshold, as shown in Fig. 1b. Notice that the rise and fall of the motor-current waveform depends on the resistance and inductance of the motor winding and is asynchronous with the PWM frequency. It is common for the waveforms during current limiting to create a periodic function with a frequency in the audible range. A chirp during startup or in response to a sudden mechanical load change is not unusual. This is generally called a subcycle oscillation and is not a cause for alarm.

Different Design Options

To illustrate different design options that integrate current-limit functionality, begin by choosing a motor that exhibits the desired mechanical performance. For this example, a low-inertia brushless motor is chosen that delivers 557 milli-Newton-meters (mNm) of torque at 2000 rpm. Also, a 48-V motor is selected with a stator winding pair whose resistance is 2.3 Ω and inductance is 2.5 mH.

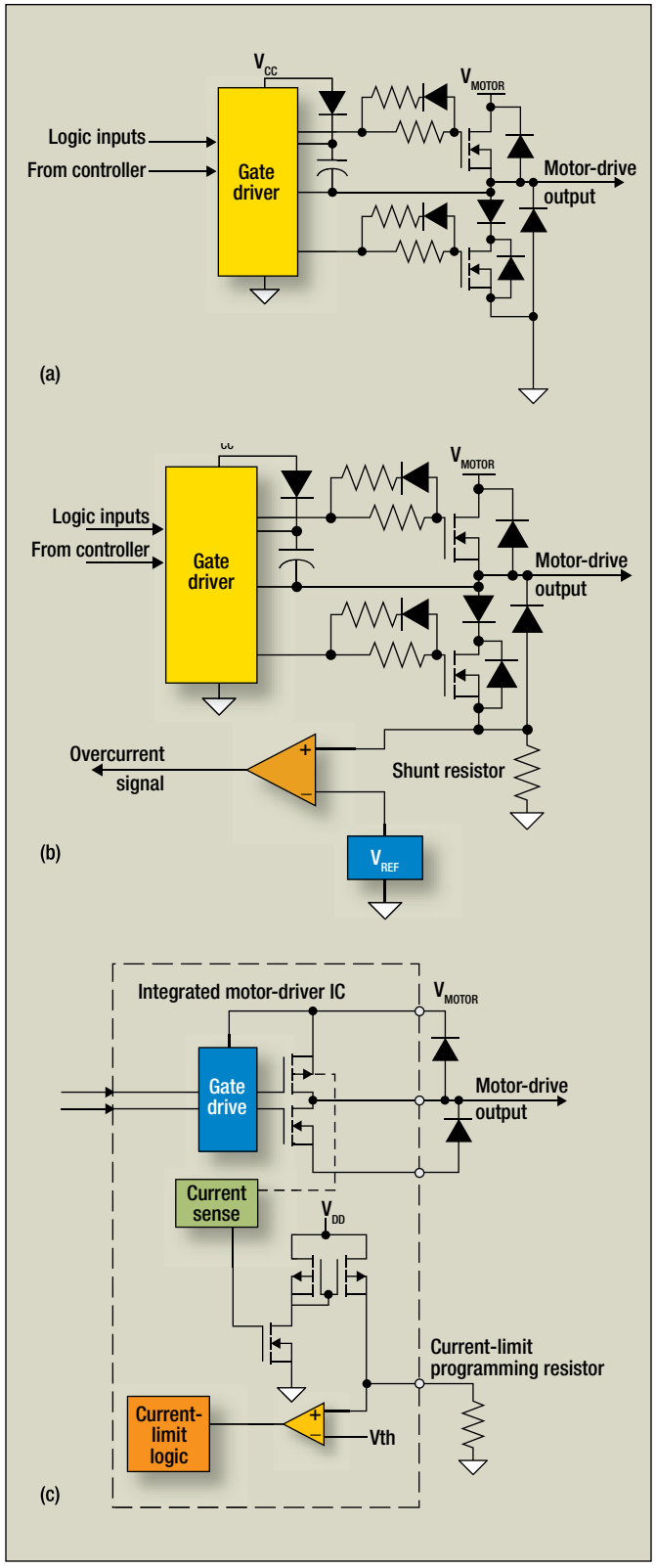

Fig. 3. *This is one phase of three different brushless dc motor-drive topologies: a brushless motor drive with a discrete output-stage design and without inrush current limiting (a), a brushless motor drive with a discrete output-stage design and inrush current limiting (b) and a brushless motor drive whose output-stage IC design has integrated current limiting (c).*

The torque constant (K_T) of the motor is 217 mNm/A. The motor-voltage constant (K_B) is 22.7 V/1000 rpm. This motor has startup currents approaching 20 A at 48 V, and there are several drive topologies to consider. In all cases, this discussion will be limited to only the output stage (the intelligent controller will be left for a different discussion).

The first approach is a topology with a discrete collection of six high-power MOSFETs and associated gate drivers that can safely handle the 20-A peak current without a current-limiting function. Fig. 3a shows one of the three phases of this topology. This approach is traditional and well documented, so it will not be discussed here in great detail. Note that the six n-channel MOSFETs are sufficient for this application and will most likely be available in a 10-mm × 15-mm D^2PAK (TO-263) or larger package. Also notice the large number of passive components that, though low in power and small, make the pc-board layout large and complex. A poor layout with this topology can lead to disastrous results.

To consider the thermal aspects of this design, the worst-case condition needs to be established for the drive's efficiency and power delivered to the motor. The peak power delivered to the motor during the nearly 20-A startup is 900 W. Assumptions must be made regarding the duty cycle of starting and stopping in the application. For purposes of this example, 95% of the life of this motor will be in continuous running mode at just under 2 A. Power dissipation for this topology will be in the neighborhood of 13 W, which is shared among the three half-bridges in the output stage.

For most n-channel power MOSFETs, the heat tab of the package is connected to the drain terminal. In a half-bridge topology, the two drain terminals are at different potentials and cannot directly share a heat-sink connection. Isolating thermal materials are the common solution for this problem, but they add thermal impedance in the path between the silicon and the heatsink. The heatsink will then need to be sized larger, with a lower thermal resistance, to make up the difference. Additionally, with a D^2PAK surface-mount package, heat will spread throughout the pc-board assembly even if the heatsink is top mounted.

The second approach extends the discrete topology further to include a current-limit function, which is fairly simple when considering only the output stage. Fig. 3b shows the modifications for only one phase. Motor current can be measured on the low side of the MOSFET stage with a precision 0.1-Ω high-power shunt resistor. All the motor current flows through the shunt resistor, developing a voltage across it. A voltage reference and comparator provide feedback to the intelligent controller, so the current-limit function can be in firmware. Some processors include the comparator and reference internally. If the current-limit threshold is set to 10 A or less, the six MOSFETs can be selected in smaller 6.5-mm × 10-mm DPAK (TO-252) surface-mount packages. The added cost and pc-board layout area of the shunt may be offset by less-expensive and smaller 10-A MOSFETs.

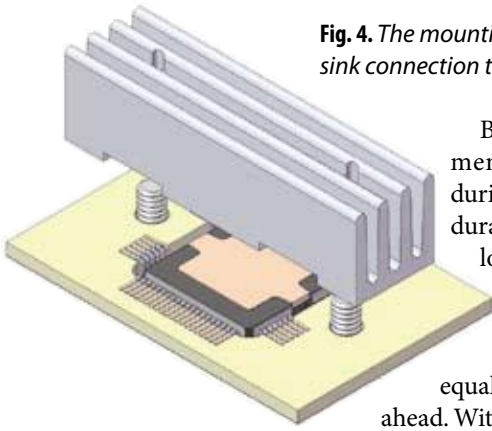

Fig. 4. *The mounting technique allows a direct heatsink connection to the motor-drive IC package.*

Because of the current-limit implementation, the power dissipation during startup will be slightly less. The duration of the starting surge will be longer because the motor will not spin up as fast, but because the power dissipation due to the on-resistance of the MOSFETs is equal to I^2R, the designer will come out ahead. With a savings of nearly 3 W, the average power dissipation for this topology is 10 W.

As discussed in the first approach, the D^2PAK surface-mount package requires an isolating thermal pad to get heat from the package to the heatsink. Thankfully, current limiting reduces the heat load by more than 25% compared with the nonlimited case.

Fig. 3c shows the third approach, which uses a single-package IC as the output stage. There are just a few three-phase brushless motor-drive ICs available today and most are limited to peak currents of much less than 10 A. However, the SA306-IHZ used in this example can handle a 17-A peak current. The 18-mm × 18-mm quad-flat pack (JEDEC MO-188) includes the six-MOSFET output stage, integrated current sensing and cycle-by-cycle current limiting. The current limit is set by the user with a ground-terminated low-power resistor. Optionally, the user can terminate the resistor into a digital-to-analog converter for dynamic control of the current-limit threshold. Unlike the current shunt used in the previous example, the current in the output MOSFETs of the IC is mirrored and provided as an analog output that reduces power dissipation in the overall circuit. The integration of the output stage, gate drivers, current measurement and current limit in one package simplifies the design, reducing the component count by more than 40 components, and the pc-board layout area is less than half of the discrete approach.

As can be seen with the discrete current-limit approach, power dissipation is lower than a nonlimited implementation. However, the integrated MOSFET of the IC will have slightly higher drain-source on-resistance, so the power dissipation of the IC design will be between the current-limited and nonlimited discrete implementations. This topology yields a total power dissipation of about 11 W.

Unlike the discrete MOSFET approaches, the IC output stage shares a common thermal surface. Most brushless motor-driver ICs are available in through-hole packaging that simplifies heatsink connections at the expense of the pc-board layout area. With the proprietary mounting technique shown in Fig. 4, the surface-mount package of the IC in this example can mate directly with a heatsink at ground potential. Eliminating the isolating thermal layer allows the heatsink to be equivalent or smaller than the discrete approaches, even though the heat load is not the lowest of the three.

The integration advantages of using an IC output stage are numerous. The layout of a pc board for a discrete design is often as challenging as the electrical design. With the convenient separation of logic-level inputs and power outputs, laying out a pc board for an IC power stage can be very straightforward. Additionally, the integration allows thermal monitoring of the output MOSFETs directly, which is difficult to implement in a discrete design, because the MOSFET packaging does not allow close proximity of a temperature sensor to each MOSFET. A discrete thermal monitor relies on accurate modeling of the thermal resistance and capacitance from the MOSFET through the package and the pc board to the sensor.

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