

## ***Reading and Interpreting Apex Microtechnology Data Sheets***

### **INTRODUCTION**

A product data sheet defines both what an amplifier can do and the conditions under which it can do it. Effective interpretation requires reading the electrical tables, footnotes, performance plots, safe operating area, and application guidance as one connected description. A voltage, current, or bandwidth headline alone cannot establish whether a device will work in a particular circuit.

This application note explains how to turn that information into design decisions. The PA85 is the reference example, while the reading method applies broadly to Apex power amplifiers. Switching amplifiers and other product families require their own device specific checks. Numerical PA85 examples refer to PA85U Rev U, April 2020 [1]. Please confirm the revision and ordered grade before applying any value to a design.

### **HOW APEX DATA SHEETS SUPPORT A DESIGN**

Begin by defining supply tolerance, output waveform and offset, load impedance versus frequency, peak and continuous current, ambient temperature, and allowable error. Include startup, shutdown, an open load, a short circuit, and energy returned by a reactive load. These conditions determine which specifications matter most.

| <b>Data Sheet Information</b>        | <b>Question It Answers</b>                                                       |
|--------------------------------------|----------------------------------------------------------------------------------|
| Equivalent schematic and connections | How does the amplifier work and how must it be wired?                            |
| Ratings and specification tables     | What are the limits and which performance values are bounded?                    |
| Performance plots and compensation   | How does behavior change with frequency, load, and circuit configuration?        |
| SOA and thermal information          | Can the output devices and cooling arrangement withstand the required operation? |
| Application and protection guidance  | What external provisions are required for reliable operation?                    |

### **EQUIVALENT SCHEMATICS AND TYPICAL CONNECTIONS**

An equivalent schematic helps identify the input stage, voltage gain stages, output devices, and protection paths. It can explain why input leakage matters, why returned load current needs a path, or why the two output polarities may dissipate power differently. It is an explanatory model; omitted parasitics and simplified bias circuits prevent it from proving every transient or fault response.

The typical connection drawing is the preferred starting reference for implementation. Trace supply bypassing, the feedback pickup point, current sensing, compensation, and signal returns before modifying the circuit. Keeping those functions visible reduces wiring errors and gives troubleshooting a known reference. A drawing is not evidence that every gain, load, or supply choice will be stable.

## PINOUT AND PIN DESCRIPTIONS

Treat the pin drawing as a mechanical interface and the description table as an electrical interface. First identify the package style, the indicated viewing direction, and the orientation reference. A bottom view mirrored onto a component side PCB layout can interchange supply and signal connections even when the pin numbers appear familiar.

**Figure 1: Compare Package Shape and Drawing Orientation Before Verifying Pins**

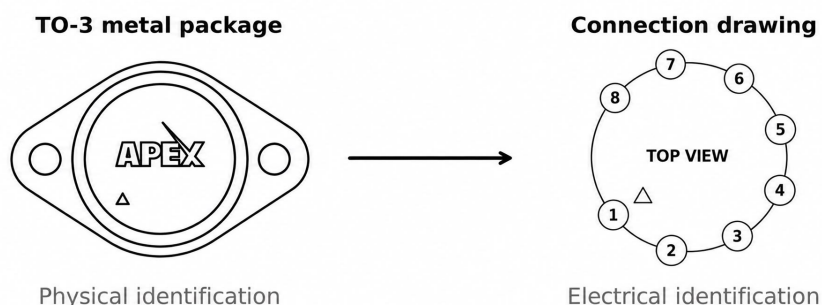


Figure 1 illustrates the comparison process, not a numbered footprint. Obtain the actual PA85 external connection drawing and CE package dimensions from Apex Microtechnology. Check mounting holes, lead locations, clearances, and the view explicitly.

| Pin | PA85 Name | Connection To Verify                                            |
|-----|-----------|-----------------------------------------------------------------|
| 1   | OUT       | Load and feedback connection                                    |
| 2   | CL        | Current sensing path through the external limit resistor to OUT |
| 3   | +VS       | Positive supply                                                 |
| 4   | +IN       | Noninverting input                                              |
| 5   | -IN       | Inverting input                                                 |
| 6   | -VS       | Negative supply                                                 |
| 7   | RC        | External compensation resistor connection                       |
| 8   | CC        | External compensation capacitor connection                      |

## READ THE DESCRIPTION BEFORE CONNECTING THE PIN

A pin name can conceal an essential connection requirement. A current limit terminal is not necessarily a logic input, and a compensation terminal is not a general purpose signal connection. Follow the device drawing for the order and location of external components. Trace the complete load current path rather than inferring it from an op amp symbol.

Also check whether a case, tab, exposed pad, or mounting surface is electrically connected or isolated. Electrical isolation does not eliminate thermal interface requirements or permit arbitrary insulating materials. Confirm the package and mounting instructions separately from the circuit diagram.

## ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings describe stress limits. They are not recommended operating points, and performance is not assured merely because a circuit remains below them. If operation results in one of these maximums being reached, no permanent damage will result. Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier. Exceeding even one rating can also cause permanent damage. There is no general allowance to exceed one limit so long as the others are respected.

Read each limit with its qualifiers. A current rating may require operation within the safe operating area. A power rating may assume a controlled case temperature. An input voltage stress limit may extend beyond the common mode range in which the input stage operates correctly. These limits must be satisfied simultaneously.

### ***SUPPLY SPAN IS DIFFERENT FROM RAIL MAGNITUDE***

For a dual supply, calculate the total span as the positive rail minus the negative rail. For example, +200 V and -200 V produce a 400 V span, not 200 V. The PA85 absolute maximum span is 450 V [1]. For a safe design, voltage rail margin should be considered to accommodate for supply accuracy, line variation, startup overshoot, ripple, and temperature dependent derating rather than placing nominal rails directly on the maximum.

### ***TEMPERATURE RATINGS DESCRIBE DIFFERENT CONDITIONS***

Storage temperature does not establish the operating range. An absolute maximum case temperature does not establish the range over which electrical specifications are met. Junction temperature describes the internal semiconductor temperature, which can, at times, be much higher than the case or ambient. It is important to use the applicable table and footnote for each different parameter check.

## READING SPECIFICATION TABLES

Before using a number, read the table heading, the row conditions, the grade columns, and every associated footnote. Record whether temperature means ambient, case, or junction. Note the supply magnitude, load value, gain, compensation, and signal amplitude. A row that overrides the general conditions takes precedence for that measurement.

| Entry                     | Design Interpretation                                                                         |
|---------------------------|-----------------------------------------------------------------------------------------------|
| Minimum                   | A lower bound under the stated conditions; useful for available swing or speed when specified |
| Typical                   | Representative behavior; useful for estimates, but not a guaranteed production limit          |
| Maximum                   | An upper bound under the stated conditions; useful for an error or dissipation budget         |
| Blank or Referenced Entry | Consult the notation. A blank is not zero, and a symbol may refer to another grade column     |

Do not combine the best value in each row into a hypothetical operating point. A fast compensation setting, a low load current swing result, and a different gain condition may describe different parametric tests and may not accurately represent specific application performance. Build one consistent set of conditions for the intended application to examine the data sheet against. This is the most effective way to understand how a device will operate under those conditions.

## INPUT SPECIFICATIONS

### OFFSET VOLTAGE AND BIAS CURRENT

Input offset voltage is the small differential input voltage needed to balance the amplifier under the specified test conditions. It is normally reported as an input referred quantity. In a closed loop circuit its contribution to output error is approximately the offset voltage multiplied by noise gain. Thus a hypothetical 1 mV offset at noise gain 20 contributes about 20 mV of output error before other errors are included.

Input bias currents flow into or out of the input terminals through the external source and feedback impedances. A useful first estimate for one path is  $V_{\text{error}} = I_B \times R_{\text{source}}$ , followed by the applicable gain to the output. Even 50 pA through 10 M $\Omega$  produces 0.5 mV. This calculation is illustrative; actual error depends on both input paths and the bias current polarities.

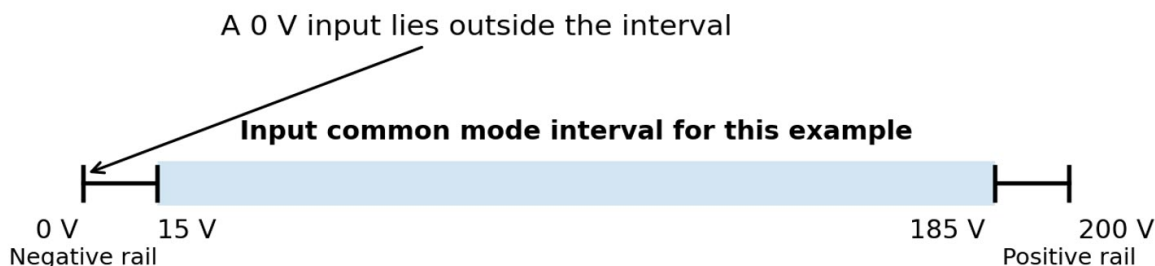
Check temperature dependence, offset current, source impedance, resistor tolerance, contamination, and leakage through protection devices. A very low room temperature bias specification does not make PCB leakage negligible. Use maximum limits and the specified temperature behavior when building the final error budget.

### COMMON MODE RANGE AND SINGLE SUPPLY OPERATION

Common mode voltage is the average of the two input terminal voltages. With negative feedback and a small differential error, both terminals usually sit near the same potential. Their common potential must remain in the specified operating interval, regardless of whether the amplifier output can approach a rail.

Using PA85 as an example, the input common mode range requires approximately 15 V of separation from each supply rail [1]. With illustrative rails of 0 V and +200 V, this translates to an input interval of about +15 V to +185 V. A ground referenced input is outside that interval. Output swing is a separate restriction and must also be checked.

**Figure 2: Applying Input Headroom to an Illustrative Single Supply Arrangement**



A noninverting input near ground cannot be assumed to work with a 0 V negative rail. An inverting circuit also requires an acceptable reference voltage at its noninverting input; calling its summing node a virtual ground does not remove the input headroom requirement. A negative rail or a suitable level shift may be needed for an Apex amplifier like the PA85 to run in a pseudo “single sided” configuration.

Evaluate the input voltages during startup, clipping, disabled operation, and an externally driven output as well as during normal closed loop operation to be sure that a common mode restriction is not having an unintended effect.

## GAIN AND OUTPUT SPECIFICATIONS

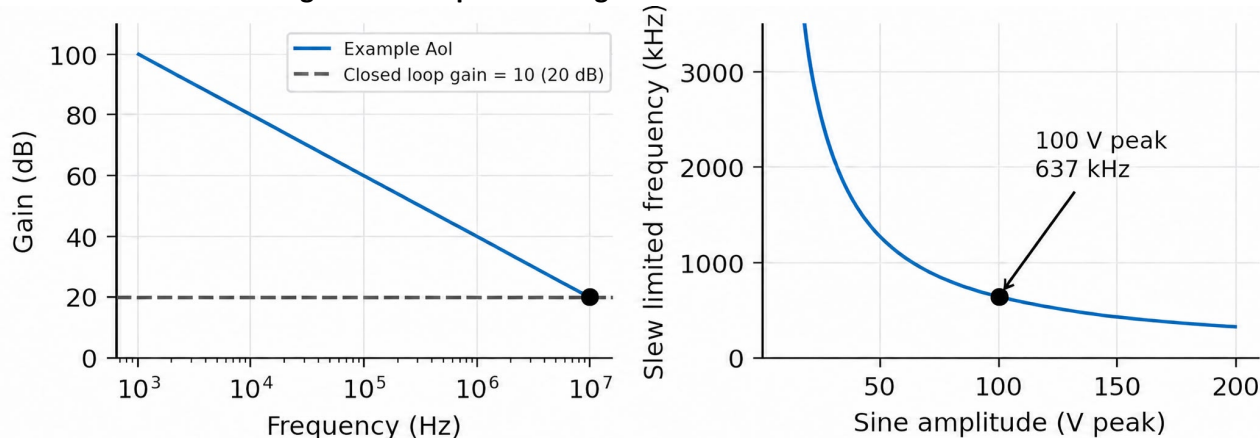
### SMALL SIGNAL BANDWIDTH AND GAIN BANDWIDTH PRODUCT (GBW)

Open loop gain ( $A_{OL}$ ) is the gain before external feedback is applied. Closed loop signal gain ( $A_{CL}$ ) is set primarily by the feedback network, only where sufficient loop gain remains. For a simple dominant pole response, the approximate closed loop bandwidth ( $BW_{CL}$ ) is the gain bandwidth product (GBW) divided by closed loop gain. External compensation and additional poles can make this approximation less accurate.

$$BW_{CL} \approx GBW / A_{CL} \quad \text{and} \quad \text{Gain in dB} = 20 \log(\text{gain in V/V})$$

A hypothetical 100 MHz gain bandwidth product and closed loop gain of 10 V/V suggest a 10 MHz crossover. On a small signal plot, 10 V/V is 20 dB. The intersection of open loop gain and the 20 dB closed gain line estimates crossover. This frequency intersection point can also be used to estimate stability of a system when correlated with the phase response ( $\geq 45^\circ$  = stable system).

**Figure 3: Example Small Signal and Slew Limited Calculations**



### POWER BANDWIDTH (PBW) AND SLEW RATE (SR)

Power bandwidth describes a specified large signal response, with amplitude, load, compensation, and distortion conditions that must be checked. Operating beyond the maximum power bandwidth for an amplifier will result in slew rate limiting as well as limited output swing capability. Slew rate limits the fastest output voltage slope. The plot above illustrates the relationship between slew rate and available operating bandwidth based on the following equations. For a sine wave, compare the required slope with the available slew rate:

$$SR_{\text{required}} = 2\pi * PBW * V_{\text{peak}} \quad \text{and} \quad PBW = SR / (2\pi * V_{\text{peak}})$$

For an example 200 V peak-to-peak sine wave and 400 V/ $\mu$ s slew rate, the theoretical power bandwidth limitation imposed by slew rate is about 637 kHz. Operating at that boundary would produce a distorted signal. Allow some margin to facilitate low distortion and check the power response plot and load current to make sure that the amplifier is capable of full output swing under load conditions. For a capacitive load example,  $I_{\text{peak}} = 2\pi f C V_{\text{peak}}$ ; a 1 nF load at 100 V peak and 100 kHz requires about 62.8 mA (6.28Wpk!).

### **OUTPUT SWING CURRENT AND SETTLING**

Use the guaranteed swing at the applicable output current rather than assuming rail-to-rail output. For example, the PA85 minimum swing at  $\pm 200$  mA is 10 V inside each rail under the table conditions [1]. Applying  $\pm 150$  V rails therefore should parametrically support a  $\pm 140$  V output swing, subject to SOA and thermal limits. Be sure to check both polarities and remember that feedback network loading can also have some effect on swing range.

Settling time includes slewing, linear recovery, and residual ringing to a specified error band. A small step settling result cannot be extrapolated directly to a full voltage reversal. Check step amplitude, compensation, load capacitance, and the required accuracy together to assure specifications are conditionally accurate for a given application.

## **POWER SUPPLY AND THERMAL SPECIFICATIONS**

### **QUIESCENT POWER AND LOAD RELATED DISSIPATION**

Quiescent current is the supply current value when no useful load power is being delivered. Its dependence on voltage and temperature must be read from the specification and plot. Quiescent current is not always proportional to supply voltage but will have some sort of characterized relationship in the datasheet. If current is approximately constant, quiescent power increases approximately in proportion to total supply span.

$$PQ \approx (+V_s \text{ rail} - -V_s \text{ rail}) \times IQ$$

As an example calculation, 21 mA across a 300 V span produces 6.3 W before load related heating. Use the relevant maximum current and temperature dependence for a worst case cooling calculation. For asymmetric voltage rail currents, calculate and sum the power from each rail instead of assuming one shared current.

For a linear output stage, an initial conduction loss estimate is the voltage across the conducting output device multiplied by its current. During sourcing, use  $(+V_s \text{ rail} - V_{\text{OUT}}) \times I_{\text{OUT}}$ ; during sinking, use  $(V_{\text{OUT}} - -V_s \text{ rail}) \times |I_{\text{OUT}}|$ . Integrate over the waveform to obtain average heating. Reactive loads can produce large internal loss while delivering little average real power to the load.

### **JUNCTION TO CASE IS ONE PART OF THE THERMAL PATH**

$$T_J \approx T_C + P_D \times \theta_{JC}$$

$$T_C \approx T_A + P_{\text{heat}} \times (\theta_{CS} + \theta_{SA})$$

Here  $\theta_{JC}$  is junction-to-case thermal resistance,  $\theta_{CS}$  is case-to-sink resistance, and  $\theta_{SA}$  is sink-to-ambient resistance.  $T_C$  must be the case temperature at the specified reference location. Adding  $P_D \times \theta_{JC}$  directly to ambient omits the rise through the interface and heatsink. Include every heat source that contributes to case or sink temperature for an accurate calculation.

| Example Output Stage Check  | $T_J$ Calculation                            | $T_J$ Result  |
|-----------------------------|----------------------------------------------|---------------|
| Case 65°C, output loss 10 W | $65 + (10 \times 4.2) = 107^\circ\text{C}$   | Below 150°C   |
| Case 85°C, output loss 18 W | $85 + (18 \times 4.2) = 160.6^\circ\text{C}$ | Exceeds 150°C |

These examples use the PA85 maximum DC junction-to-case value of 4.2°C/W and its 150°C junction stress limit [1]. The passing example is only a thermal screening result; it does not establish SOA compliance or sufficient life margin. A practical design should target a lower junction temperature and account for measurement and modeling uncertainty.

The PA85 distinguishes output stage dissipation from additional quiescent heating in its rating notes [1]. Preserve that accounting: use the output stage loss for its junction rise and derating check, and include total package heat when calculating case and heatsink temperatures. Do not assume all internal heat originates at one equivalent junction, although dissipation will be dominated by the output when an amplifier is delivering current to the load.

Use an AC thermal rating only when stated input conditions for alternating conduction (AC) between output devices are met. A high frequency signal with a large DC offset may continue to heat one device disproportionately. Neither an average package power check nor a large heatsink replaces the SOA check, which will be explained in a later section.

## TYPICAL PERFORMANCE GRAPHS

Typical plots explain trends and help select initial component values. They do not create new guaranteed minimum or maximum specifications. Before reading a curve, check both axes, units, logarithmic scales, curve labels, temperature, supply span, load, gain, and compensation conditions listed. Interpolation within the plot is an estimate, while extrapolation outside the plotted conditions requires additional evidence.

Compare the plot conditions to the table conditions before concluding that two results disagree. For example, a bandwidth curve with one compensation capacitor cannot be combined with a phase curve for another capacitor. A slew rate or current limit graph can reduce initial design iterations, but **it cannot replace verification at the required tolerances and operating extremes.**

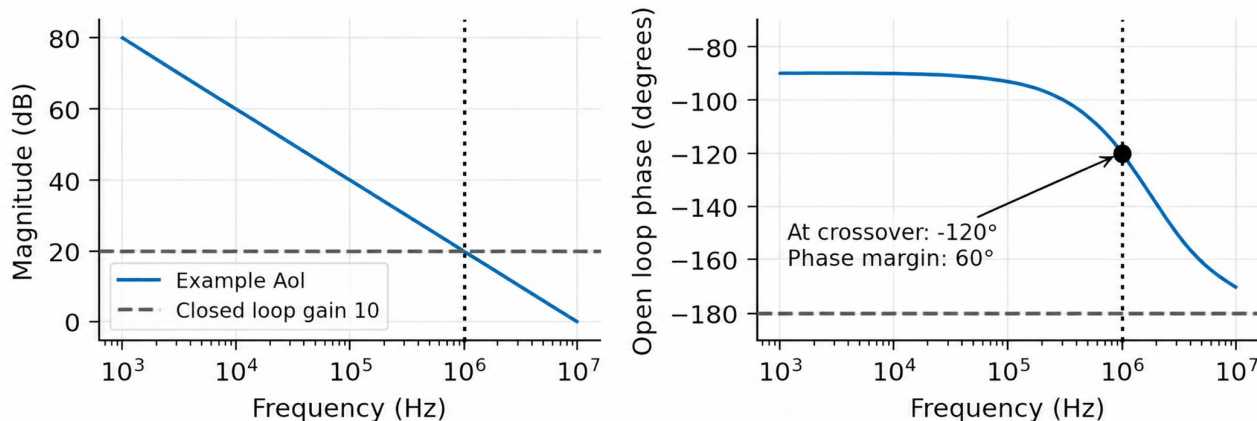
## USE CLOSED LOOP GAIN WHEN EVALUATING STABILITY

Loop gain is  $T = A_{OL} \times \beta$ , where  $\beta$  is the fraction of output returned to the error input with independent signal sources set to zero. Closed loop gain is  $A_{CL} = 1/\beta$ . For a simple non-inverting resistive circuit,  $A_{CL} = 1 + R_F/R_{IN}$  and equals signal gain. For a simple inverting circuit, signal gain is  $-R_F/R_{IN}$  while AC gain is still  $= 1 + R_F/R_{IN}$ . An inverting gain of -1 therefore has AC gain of 2.

For example, plot closed loop gain against open loop gain. At their intersection, loop gain magnitude is unity. Read the corresponding phase using the same compensation and loading conditions. If the feedback

factor has negligible phase shift there, the phase margin is approximately  $180^\circ$  plus the negative open loop phase angle.

**Figure 4: Example Crossover and Phase Margin Construction**



The example crosses at 1 MHz with open loop phase of  $-120^\circ$ , giving about  $60^\circ$  phase margin for a resistive feedback network.

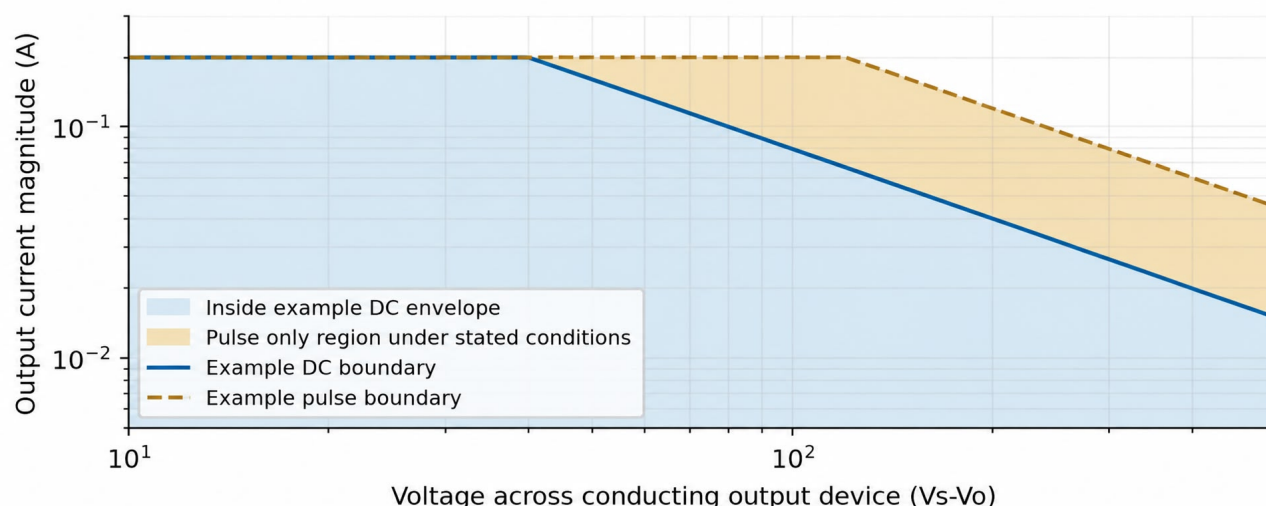
Phase margin of greater than or equal to  $45^\circ$  is often a preliminary design target, however it is not a universal pass criterion. Load capacitance, wiring, compensation tolerance, output isolation components, and multiple trace or wire crossings can change stability. Confirm the complete circuit with appropriate loop analysis and bench step testing. Examine ringing and recovery with the actual load across supply and temperature conditions to be sure of a design configuration.

## SAFE OPERATING AREA

The safe operating area defines allowed combinations of output device voltage, current, temperature, and exposure time. It is more restrictive than independently checking the maximum output current and maximum supply voltage. A given point can satisfy both specified voltage and current ratings and still exceed an output device heating limit.

On a supply-to-output differential axis, use the voltage across the conducting output device. For a sourcing device this is approximately  $+V_s$  rail -  $V_{OUT}$ . For a sinking device it is approximately  $V_{OUT}$  -  $-V_s$  rail. The horizontal coordinate is not simply the output voltage relative to ground.

Figure 5: Conceptual DC and Pulse Regions with Illustrative Boundaries



The blue shading illustrates combinations below a DC boundary; the amber shading adds combinations available only under a pulse boundary.

### ***FOLLOW THE ENTIRE LOAD TRAJECTORY***

As an example case, +150 V supply, +100 V output, and 100 mA sourced current put about 50 V across the sourcing device and produce 5 W of instantaneous conduction loss. At 0 V output with the same sourced current, the device instead supports 150 V and dissipates 15 W. Equal output current does not imply equal device stress.

Plot the trajectory for both output polarities and include transients. A capacitive load draws its greatest sinusoidal current near a voltage zero crossing; current may also continue while the output changes polarity. An inductive load can return energy into a supply. Check these trajectories rather than considering only the output waveform peaks to be fully aware of all power dissipation possibilities.

### ***A PULSE CURVE IS CONDITIONAL PERMISSION***

A pulse envelope cannot be treated as a continuous operating limit or converted into a repetitive pulse rating solely by scaling average power. Pulse duration, repetition, initial temperature, thermal recovery, and any transient thermal guidance will all have an effect. If the data sheet does not define the required repetitive condition, obtain manufacturer guidance or use the applicable continuous boundary conservatively in order to preserve the amplifier output stage function.

During a short circuit, current limiting can hold the output devices at a particularly demanding voltage-current point but does not always engage quickly enough to provide absolute protection. Check the sustained fault at the selected limit and maximum case temperature. Passing the SOA trajectory and passing the overall heatsink calculation are both required for full confidence.

## TYPICAL APPLICATION AND PHASE COMPENSATION

Read the typical application for transferable design details even when the end use differs. Trace signal summing, DC bias, feedback pickup, bypassing, protection, and component voltage ratings in order to see if anything can be useful. Determine which values are essential to the amplifier and which are selected for the example load. A typical application illustrates a method; it is not a tested design for every proposed substitution.

External compensation trades speed against stability. Use the device compensation guidance as the starting point and then evaluate the actual noise gain, its variation with frequency, and the load. Signal gain alone can be misleading for an inverting stage or a circuit with reactive feedback.

| PA85 Listed Gain [1] | CC     | RC           |
|----------------------|--------|--------------|
| 1                    | 68 pF  | 100 $\Omega$ |
| 20                   | 10 pF  | 330 $\Omega$ |
| 100                  | 3.3 pF | 0 $\Omega$   |

These are the three entries published in the PA85 phase compensation table, not a general interpolation rule. Follow its connection diagram and voltage rating requirements. The PA85 stability guidance specifies a 500 V working voltage compensation capacitor and close placement at pins 7 and 8 [1]. The array of compensation capacitor values mentioned in the example show that, at picofarad values, PCB parasitic capacitance and probe loading can have significant effect on circuit performance.

## CURRENT LIMIT

Current limit behavior is device specific. Some Apex products use a resistor, while others use a different mechanism or require external protection. Use the equation from the specific product data sheet rather than transferring a rule from a similar part. For the PA85, the published equation [1] can be rearranged as:

$$RCL = 0.7 \text{ V} / (ICL - 0.016 \text{ A})$$

$$ICL = (0.7 \text{ V} / RCL) + 0.016 \text{ A}$$

For an example 100 mA setting,  $RCL = 0.7 / (0.100 - 0.016) = 8.33 \Omega$ . A nominal 8.2  $\Omega$  value predicts about 101 mA. This is a nominal estimate. To be extra safe, use the typical curve, temperature behavior, resistor tolerance, and verification measurements to establish a suitable design margin.

The PA85 guidance gives a 1.4  $\Omega$  minimum resistor and 30  $\Omega$  maximum practical value [1]. The equation therefore cannot be extrapolated to arbitrarily low current. At 30  $\Omega$  it predicts approximately 39 mA. A requested 2 mA limit cannot be achieved using this resistor equation alone. It is important to understand that standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow  $\pm 20\%$  variation at room temperature. Furthermore, the current limit varies over temperature.

For resistor heating, use  $I_{RMS}^2 \times R_{CL}$  during normal operation and check its pulse and sustained fault ratings. Evaluate voltage rating, temperature coefficient, inductance, and physical placement. **Current limiting reduces current; it does not automatically protect against excessive dissipation, every transient, or prolonged operation outside SOA.**

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## **PROTECTION RECOMMENDATIONS**

Evaluate every protection recommendation against the fault source, energy, duration, and amplifier connections.

### ***INPUT AND SUPPLY PROTECTION***

Check input protection during overdrive and loss of feedback. Limit differential stress without introducing unacceptable leakage, capacitance, or recovery behavior. Provide a controlled clamp current path and select components for source impedance and fault energy.

Supply protection must address startup overshoot, polarity reversal, and returned load energy. The PA85 identifies negative rail opens or reversals as potential input stage failure conditions [1]. Place protection and bypass paths close to the pins. Check TVS diode standoff voltage, clamping voltage at actual current, energy, temperature, and repetitive operation.

### ***REACTIVE LOADS AND PHYSICAL IMPLEMENTATION***

Provide a path for inductive flyback and returned energy. Verify that the supply can absorb this energy or that an external network can dissipate it.

Review mounting, thermal interfaces, bypass placement, and feedback routing. Use controlled discharge procedures and measurement equipment rated for the voltage and energy required with some added margin. Follow handling precautions and never open or mechanically process sealed hybrid packages.

## **READING COMPREHENSION**

Keep a design record that links each requirement to its supporting row, footnote, curve, or application paragraph. Record the revision and ordered grade of a product. Use typical values for estimates and specified limits for the applicable worst case checks.

Before release of a design, verify worst-cased input excursions, output swing and current, speed and settling, compensation and load, junction temperature, and SOA. Repeat checks for startup, shutdown, and credible faults. Use simulation to examine interactions and bench measurements to confirm the actual load and cooling arrangement.

For conditions not covered, contact Apex support with the schematic, supply limits, waveform, load model, and thermal measurements.

## REFERENCES

1. Apex Microtechnology, PA85 and PA85A High Voltage Power Operational Amplifiers, PA85U Rev U, April 2020. Refer especially to pp. 3–6 and 7–12. <https://www.apexanalog.com/resources/products/pa85u.pdf>
2. Apex Microtechnology, AN56 Ultra High Voltage Unity Gain Buffer, Rev A, May 2016. Used as the document layout reference.

PA85 product and document access: <https://www.apexanalog.com/products/pa85.html>. Reference revision reviewed October 26, 2026. Numerical examples and conceptual plots in this note are instructional calculations unless explicitly identified as published PA85 data.

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## NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

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