Ultra High Voltage Unity Gain Buffer

INTRODUCTION

When designing a system using high voltage amplifiers, it is necessary to protect the amplifier and other components in the system. In many multiple stage analog systems, unity gain buffers are commonly used to isolate one stage from the other. It is also used to measure the output of an analog circuit, without loading the circuit.

In essence, a buffer does not need to be set at unity gain. It can have a gain of some value, or set to unity gain depending on the requirement and circuit design. Application note AN52 describes a high voltage unity gain current buffer. This application note details the design of a high voltage unity gain buffer using N-channel MOSFETs and some passive components that can be used as a voltage follower circuit.

A unity gain buffer or unity gain amplifier is basically an operational amplifier set at unity gain. Just like a regular op amp, a unity gain buffer amplifier provides high input impedance and low output resistance. The buffer can be used to isolate two stages, where the input of the buffer is connected to the output of the first circuit, and the output of the buffer is connected to the input of the second circuit. The input current of the buffer is essentially zero (in pico Amps), just the leakage current of the MOSFET in the circuit. This way, the voltage of the first circuit remains undisturbed and can be measured at the output of the buffer.

TYPICAL VOLTAGE FOLLOWER TOPOLOGIES

A simple unity gain voltage follower can be constructed using a stable unity gain amplifier as shown in Figure 1. The amplifier is operated in the non-inverting mode and the gain is set to 1. The output voltage will be the same as the input voltage. The high input impedance for a buffer is established by the high input impedance of the particular op amp. Likewise, the low output impedance requirement of the buffer is set by the output stage of the op amp.

Figure 1: Voltage Follower

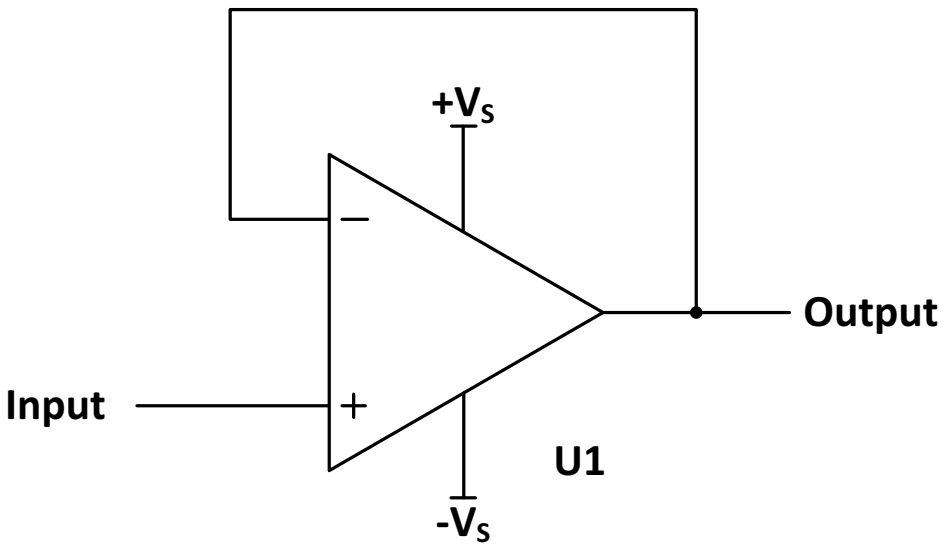
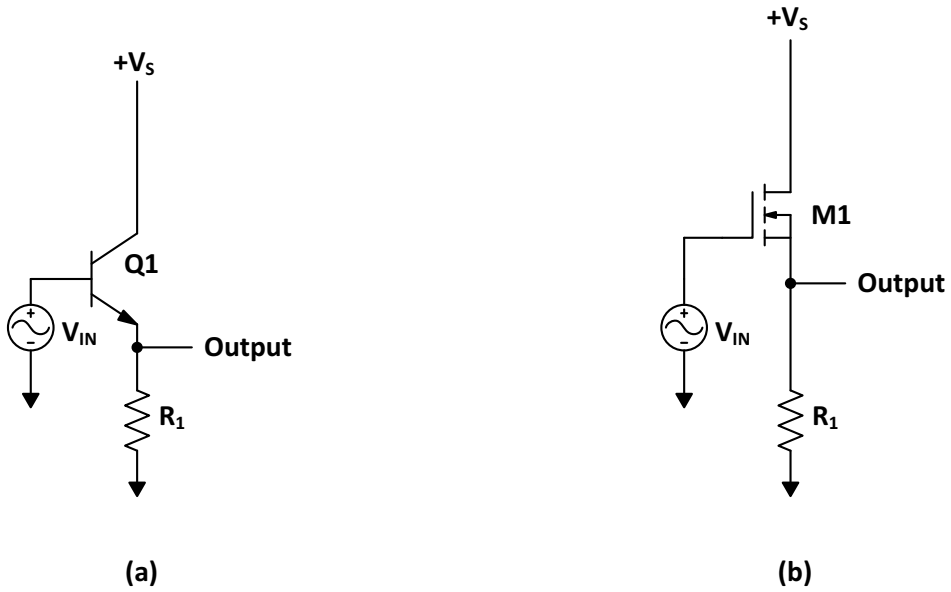


Figure 2 (a) shows a voltage follower using a BJT, also called an emitter follower circuit. In the circuit, the collector is connected to a common voltage (or supply voltage), the base is used as the input and the output is measured at the emitter of the transistor. Once the transistor is ON, the Emitter will provide the same signal level as present at the Base. This circuit can be further developed by using a MOSFET as a source follower circuit, as shown in figure 2 (b). A MOSFET is preferred as it provides a higher input impedance than a BJT and can be used for higher voltages. In a source follower circuit, the input is connected to the gate of the MOSFET and the output is measured at the source of the MOSFET, similar to an Emitter follower circuit. The drain of the MOSFET is connected to the supply voltage.

Figure 2: Voltage Follower using BJT and MOSFET

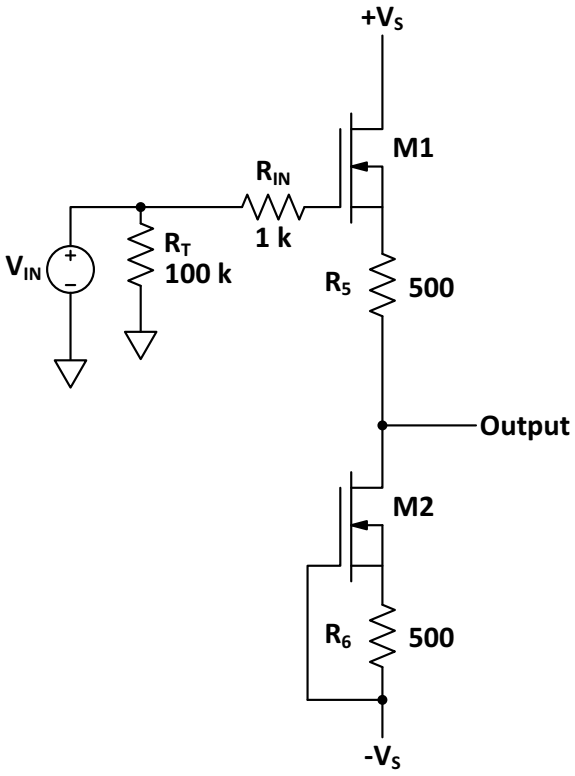


The design of the high voltage unity gain buffer in this application note is developed on the idea of using a source follower as a voltage buffer.

HIGH VOLTAGE UNITY GAIN VOLTAGE FOLLOWER

This section describes the design of a high voltage follower circuit based on the voltage follower circuit shown in figure 2 (b). A simplified circuit diagram of the voltage buffer is shown in figure 3. The circuit consists of two depletion mode MOSFETs M1 and M2. Depletion mode MOSFET M2 is configured as a constant current source. The desired bias current of the MOSFET stage can be set by adjusting R6 resistor. Note, the gate of M2 is connected to the negative supply, and so is R6. This sets them both at the same potential. Depending on the MOSFET, R6 may not be necessary (if Idss of the MOSFET is the bias current you require). Assuming M1 is the same as M2, the output voltage at the drain of M2 then is equivalent to the gate voltage at M1 (since the MOSFETs have the same transfer characteristics and the same bias current). The input signal is connected to the gate of M1 and the output is connected at the drain of M2. In this configuration, we force the Vgs of M1 to be equal to Vgs of M2. Rt resistor at the input is used only during testing of the circuit. It is not required as the gate of the MOSFET has a higher input impedance. The complexity of biasing the current for the output stage is reduced when using a depletion mode MOSFET, which makes it a simple design. When the power supplies are switched on, both M1 and M2 are switched on. Resistor R6 sets the bias current for the circuit. The bias current flows from +VS to –VS.

Figure 3: Conceptual Design



There are a few limitations to using the conceptual design for high voltages without adding any other components. The voltage capability of the circuit is limited by the maximum Vds of the high power depletion mode MOSFETs available. Since the most readily available high power depletion mode MOSFETs have a Vds of 1000 V, we used high power enhancement mode MOSFETs in cascode with M1 and M2, to share the voltage drop and the power dissipation.

ACTUAL PROTOTYPE

The actual circuit used for prototyping is shown in figure 4. A PA99 power amplifier is used to provide the required high voltage of 2 kV p-p to the unity gain buffer. The PA99 is set at a gain of 200, in a non inverting configuration. The PA99 provides an output voltage of 2 kV p-p, which is then used as an input to the voltage buffer.

The voltage buffer circuit consists of two enhancement mode MOSFETs M1 and M3 (IXTA02N250HV) that are used to share the voltage drop across the depletion mode MOSFETs M2 and M4 (IXTP3N100D2). This is a typical cascode amplifier stage which allows us to extend the voltage range of the circuit. MOSFET (N-channel depletion mode) M4 and resistor R6 form the current source of the circuit. The operating point set at the source of M2 will be equal to operating point set at the source of M4. Resistors R5 and R6 are used to set the bias the current through the MOSFETs. The bias current is set according to the formula:

$$I = \frac{Vgs}{R_6}$$

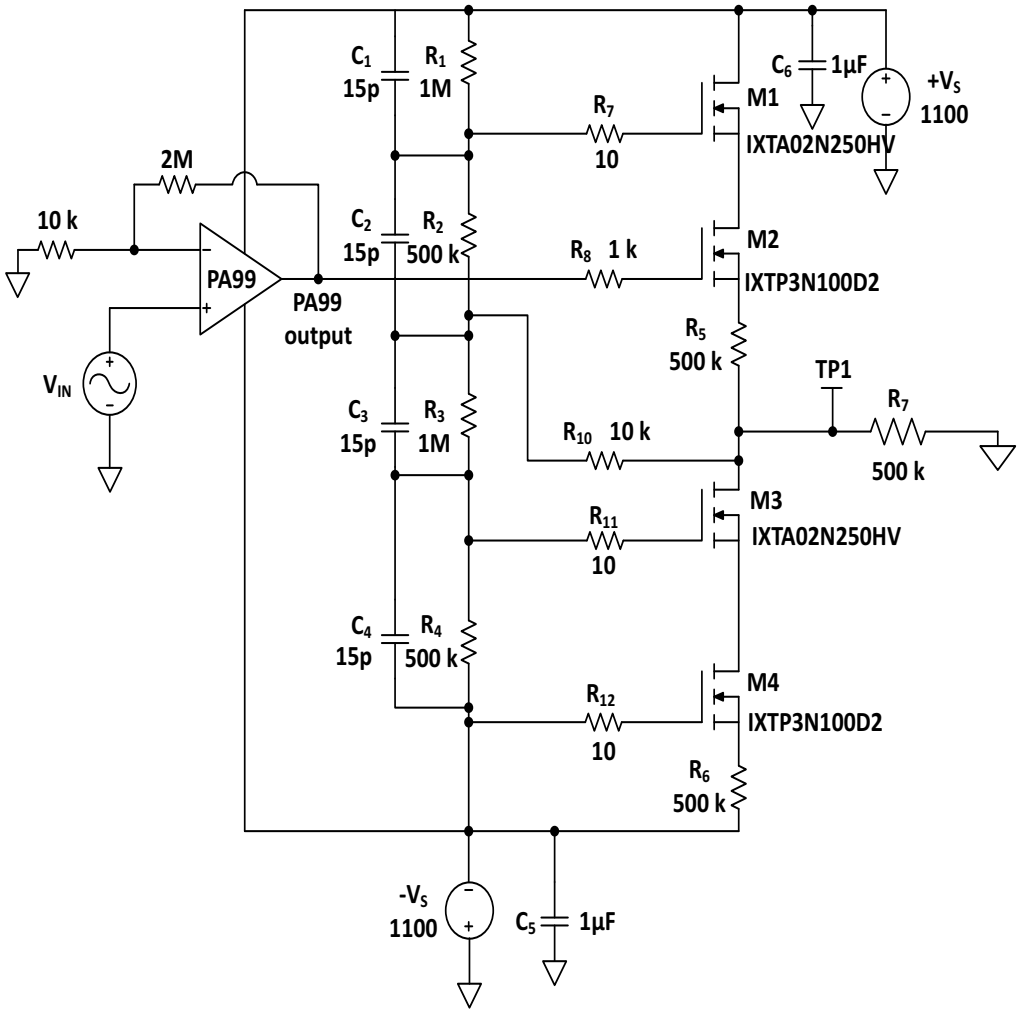
Where Vgs is the gate to source voltage of M4. The transfer characteristics (or the input admittance characteristics) of a MOSFET are used to calculate the required drain current. The bias current in the MOSFETs is

set to 6 mA for a Vgs of approximately -2.8 V. Since the gate and source of M4 are connected to the same node, they will be at the same potential.

To explain the working of the current buffer circuit, let us assume that the input signal is zero volts. This means the gate of M2 will be at zero volts. R1, R2, R3 and R4 are in series across the power supplies. Their function is to establish voltage drop for the Vds of each of the MOSFETS. They can be scaled such that the MOSFETs with higher voltage rating share larger portion of the total voltage. The voltage at the source of M2 will be then slightly less than zero volts as long as M2 is conducting. The positive and negative supply voltages are set to +/- 1100V. Since R2 and R4 are set at same value, the voltage drop across these resistors (and across M2 and M4) will be same. Now, if there is an input voltage of 1000 volts to the buffer circuit (gate of M2), the voltage at TP1 will be 1000 V. This means there will be a voltage drop of approximately 100 V (+1100 - 1000) across MOSFETs M1 and M2. Since the negative supply is set at -1100 volts, the voltage drop across MOSFETs M3 and M4 will be approximately 2100 (-1100 - 1000). R10 is a bootstrap resistor.It is used to provide the desired voltage drops across R1, R2, R3 and R4. With proper biasing of the resistors R1, R2, R3 and R4, as shown in the figure, the voltage drop across each MOSFET (Vds) can be set to a particular value. In this case, we set the resistors in a way that the enhancement mode MOSFETs M1 and M3 share higher voltage than the depletion mode MOSFETs M2 and M4. With the output at 100 V, M1 would have a Vds of approximately 78 V and M2 will have a Vds of approximately 22 V. This way, the Vds drop across M3 will be approximately 1.4 kV and the Vds voltage drop across M4 will be approximately 700 V. If all the four resistors are set to an equal value, they will share equal voltage across them.

Capacitors C1, C2, C3 and C4 are used to balance the voltage drops across the resistors during transient conditions. Resistors R7, R11 and R12 are used in series with the MOSFETs gate to prevent instability due to oscillations in the circuit. Capacitors C5 and C6 are used as bypass capacitors to prevent noise from the power supply. The bypass capacitors need to be rated for the total supply voltage (+Vs to -Vs). A 15 µF 3kV ceramic capacitors are used for each supply to reduce power supply noise.

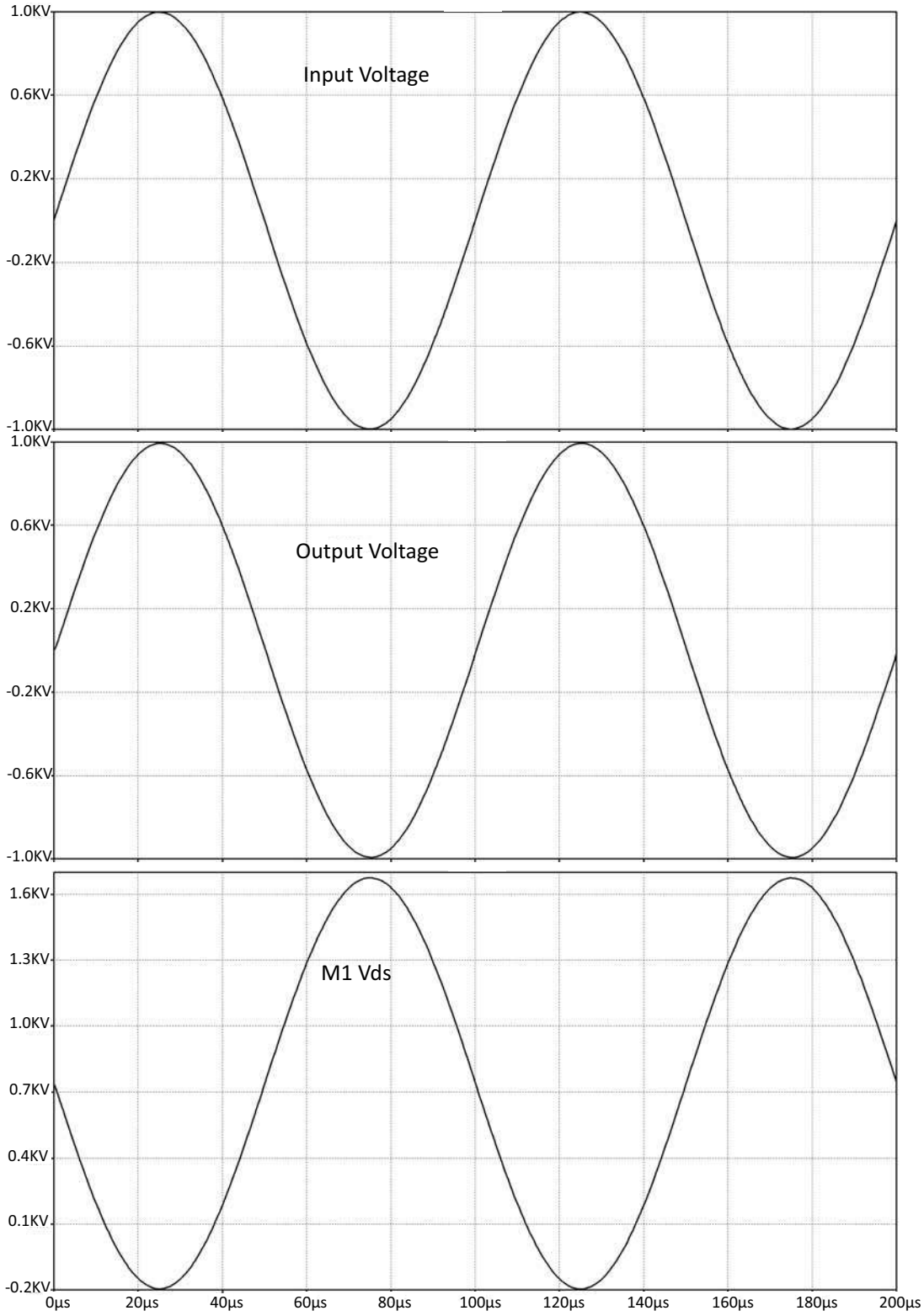
Figure 4: Actual Prototype Circuit

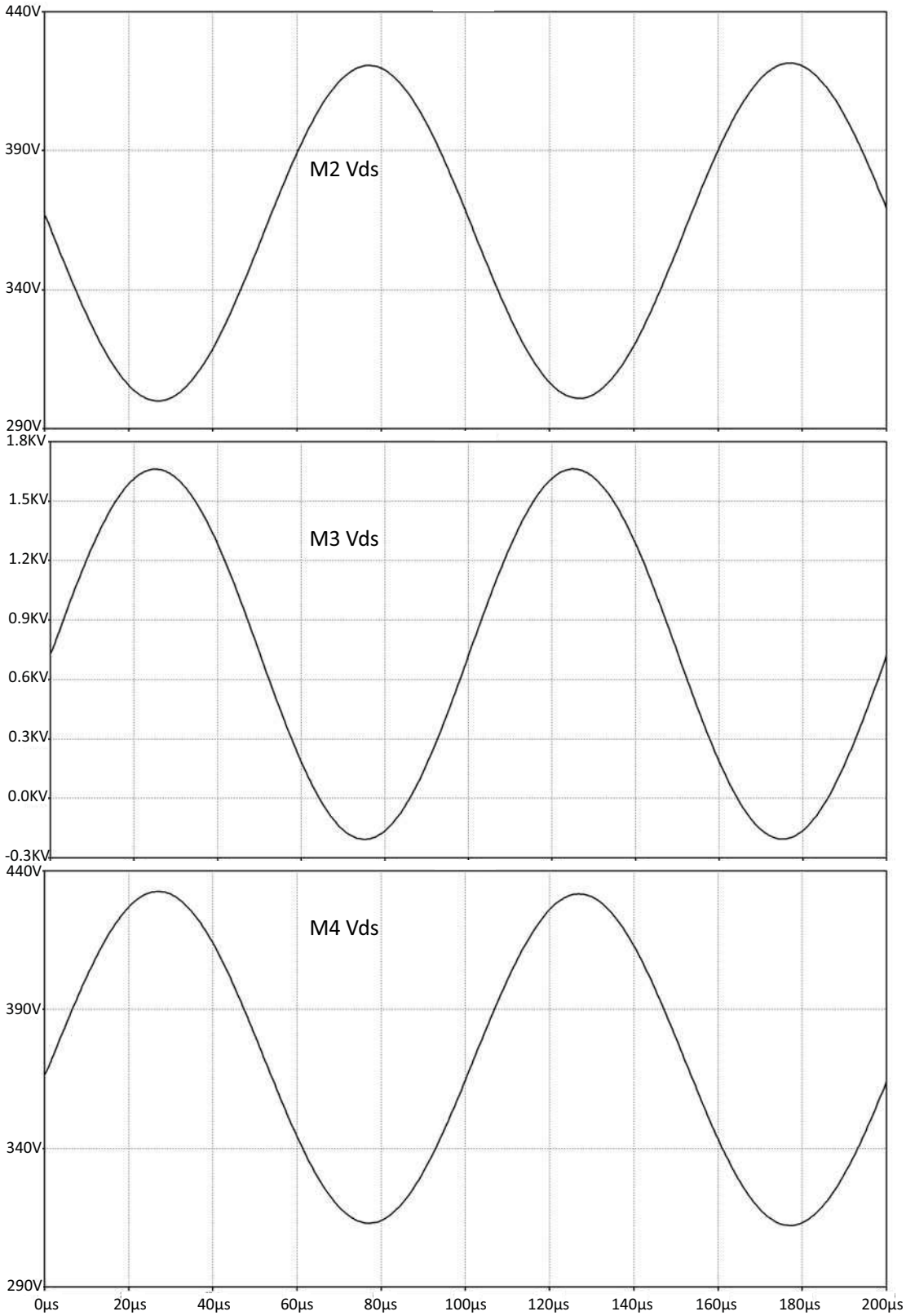


The circuit was tested for an operating voltage of 2 kV p-p sine wave. The input to the buffer was provided using a PA99 amplifier as shown in figure 6. The input signal was tested at frequencies up to 10 kHz. When the input is swinging from +1000 V to – 1000V, the calculations for Vds drop across the MOSFETs changes. The maximum Vds drop across M1 and M2 combined will occur when the output voltage level is at -1000V. when the output voltage hits -1000V, the total voltage drop across M1 and M2 is 2.1 kV. The Vds across M1 is then 1.67 kV and Vds across M2 is 430 V. Similarly, the maximum Vds drop (2.1 kV) across M3 and M4 will occur when the output voltage level is at +1000V.

The simulation waveforms in figure 5 illustrate circuit operation under light load conditions. The input voltage is 2 kV p-p, and the output voltage is also 2 kV p-p across a 500 kΩ load. The plots also show the Vds voltage drop across MOSFETs M1 and M2 in relation with the output voltage. The plots can be used to understand the voltage drop across each MOSFET and to calculate the power that is being dissipated in them.

Figure 5: Stimulation Waveforms for a Sine Wave Input



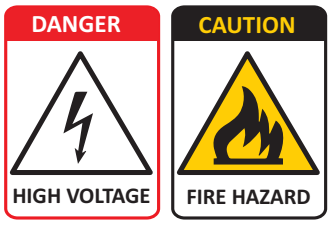

440V
390V
340V
290V
M2 Vds
1.8KV
1.5KV
1.2KV
0.9KV
0.6KV
0.3KV
0.0KV
-0.3KV
M3 Vds
440V
390V
340V
290V
M4 Vds
0µs
20µs
40µs
60µs
80µs
100µs
120µs
140µs
160µs
180µs
200µs

The advantages of this topology are:

1. Simplicity in designing the circuit because of Depletion mode MOSFETs
2. Few components required
3. High operating voltage range due to cascode stage
4. Inherently stable as there is no feedback loop

SAFETY PRECAUTIONS

When operating the circuit under high voltage conditions, it becomes very easy to damage the circuit components. Therefore it is very important to observe proper safety precautions when working under these conditions. Ensure that the MOSFETs are properly attached to a heatsink. Since these MOSFETs are subjected to very high voltages, considerably large amount of power gets dissipated across the MOSFET. The silicon pads used between the MOSFET's heat tab and the heatsink needs to have a high temperature coefficient. The used silicon pads should have a high isolation voltage that changes with temperature as little as possible. For, if the isolation breaks down, the MOSFET's drain can be shorted to the heatsink.



The non-insulated high Voltages that are present when operating the voltage follower at high voltages constitute a risk of electric shock, personal injury, death and/or ignition of fire.

REFERENCES

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