External Current Limit for Apex Power Op Amps

INTRODUCTION

Apex AN09, “Current Limiting”, discusses the basic internal current limit function of Apex operational amplifiers. Although most Apex op amps have a built-in current limit function, some devices (like PA107, PA74/PA76 or PA75) will require external circuitry when current limit function is needed. This article will discuss some possible solutions with simulation and lab test results.

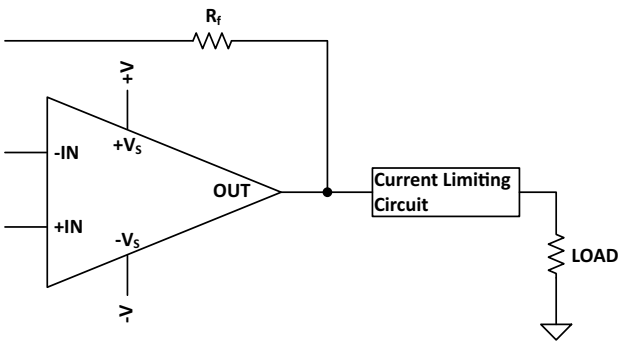
EXTERNAL CURRENT LIMIT CIRCUIT LOCATIONS

With the objective of delivering desired power to the load and reducing the risk of violating the op amp’s SOA, the external current limit circuit can be placed either at the output of an application, or at the power supply rails of the op amp.

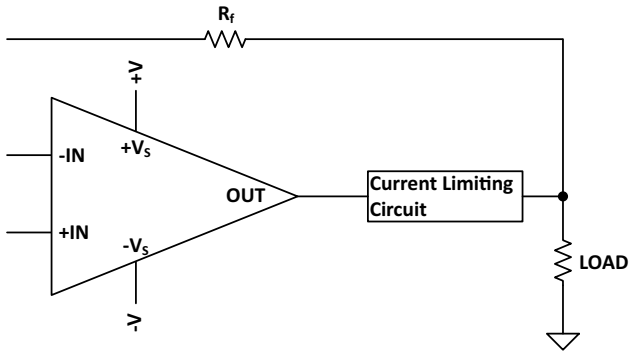
When placed at the output of an application, a current limit circuit can be located either outside of the op amp’s closed-loop (Figure 1a), or inside of the closed-loop (Figure 1b). The maximum current limited by the current limit circuit will be the same for both configurations, with slightly different behaviors.

Figure 1: Current Limit Circuit at Output

A.) Current limit circuit located outside the closed-loop



B.) Current limit circuit located inside the closed-loop

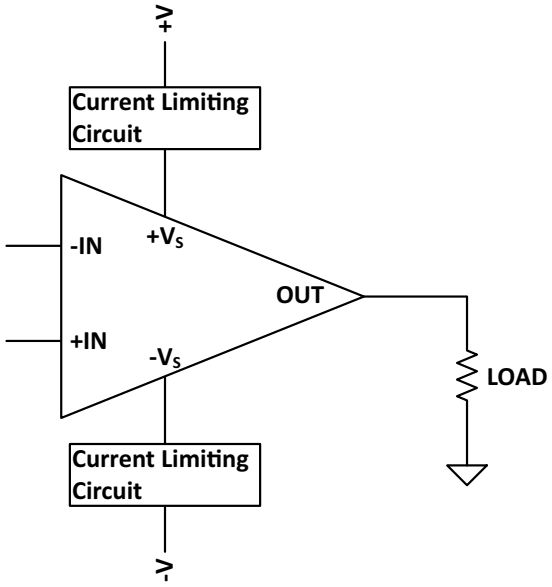


The first connection allows the op amp circuit to be designed as normal without a current limit circuit and then add the current limit circuit. The final system will have the same original performance of the op amp circuit (in term of frequency response, phase shift, etc.), with a slightly lower output voltage delivered to the load which is caused by the voltage drop of the current limit circuit. This configuration is also good for adding a current limit circuit to an existing system. It can be designed as a 2-terminal component and inserted between the op amp’s output and the load without re-spinning the main system board.

If the load requires a precise voltage, and the voltage drop caused by the current limit circuit is not acceptable for the application, the configuration in Figure 1b can be used. With the current limit circuit included in the closed-loop, the voltage drop across the current limit circuit will be compensated by the system, but the characteristics of the circuit could be different from the original circuit. Therefore, the stability and other performance of the new system should be evaluated.

When placed at the power supply rails (Figure 2), the current limit circuits will limit the current provided to the op amp which also means lower the supply voltages to the op amp.

Figure 2: Current Limit Circuit in the Supply Rails



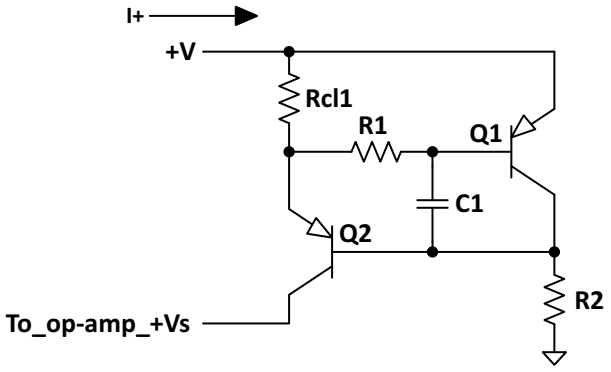
EXTERNAL CURRENT LIMIT CIRCUIT TOPOLOGIES

BJT CIRCUIT FOR EXTERNAL CURRENT LIMITING

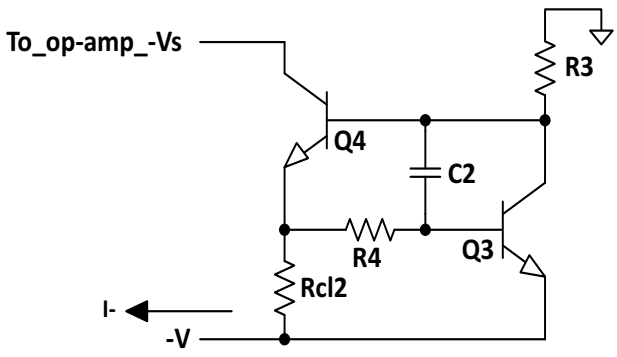
In 1991 Apex introduced a BJT based circuit for external current limit function, as shown in Figure 3. Two circuits are used as current limit circuit and are inserted between the op amp's power supply pins and the supply rails. The circuits operate in the same way as built-in current limit circuitry, as discussed in AN09.

Figure 3: Typical BJT Current Limit Circuit

A.) BJT positive rail current limit circuit



B.) BJT negative rail current limit circuit



N-CHANNEL DEPLETION MODE MOSFETS FOR EXTERNAL CURRENT LIMIT CIRCUIT

The BJT transistors in Figure 3 can be replaced by N-channel Depletion Mode MOSFETs to build a simpler current limit circuit as shown in Figure 4. Unlike Enhancement Mode MOSFETs, which are "normally-off" devices, Depletion Mode MOSFETs are "normally-on" and stop to conduct when V_{GS} exceeds a certain value.

This makes it possible to work as a simple normally-on current limit circuit. With the low $R_{DS(on)}$ (Drain-Source ON resistance) of today's MOSFETs, the circuit will be more efficient with lower power losses and lower supply voltage drops.

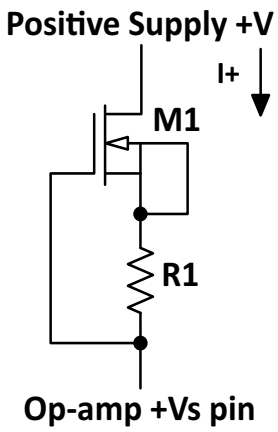
In figure 4, the current limit circuit for both positive supply and negative supply can use the same circuit/components to provide a symmetrical limit for sourcing and sinking output current. The R1 and R2 also can be selected with different values if an application requires different limit for sourcing and sinking output currents.

The Depletion Mode MOSFET in the circuit will function as a normally on-switch. For the positive supply side circuit (Figure 4a), when supply current I+ is small, M1 is fully on and the current will flow to the op amp's +Vs pin . As the current increases, the voltage across the current sense resistor R1 will increase which makes the V_{GS} of M1 more negative towards its $V_{GS(off)}$ level. Starting from this point, the MOSFET will try to limit the current flowing between its Drain and Source, until the current I+ reaches a dynamic balance at the designed maximum value.

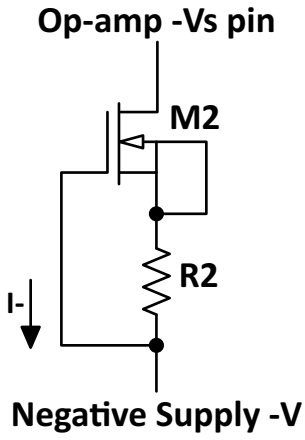
For the negative supply (Figure 4b) the circuit works in the same way as the positive supply however with opposite connections for the op amp pin and supply rail.

Figure 4: 4 N-Channel Depletion Mode MOSFET Current Limit Circuit (at Supply Rails)

A.) MOSFET positive rail current limit circuit



B.) MOSFET negative rail current limit circuit



The voltage drop of each current limit circuit can be estimated using Equation 1 Voltage Drop of a Supply Rail Current Limit Circuit. The maximum available voltage to the op amp is V_S - V_{DROP}.

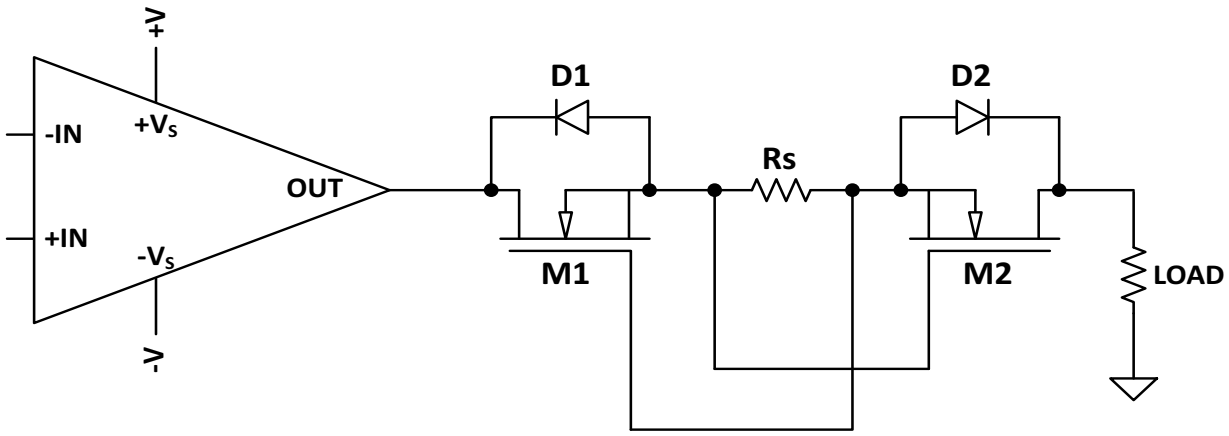
Equation 1: Voltage Drop of a Supply Rail Current Limit Circuit

$$V_{DROP} = I \cdot (R_{DS(ON)} + R_{GS})$$

Where R_{GS} is R1 or R2 in Figure 4

The circuit in Figure 4 can be considered as a "Passive" two-terminal equivalent component without the power and ground connections. This will make it possible to build a bi-directional current limit circuit with shared current sense resistor (R_S), and placed at the output of an application, as shown in Figure 5.

Figure 5: Bi-Directional Current Limit Circuit at Output



When the output current is positive, flowing from left to right (sourcing current), M1 and R_S create a current limit circuit and D2 will short the Source and Drain of M2 with about 0.7V voltage drop.

When the output current is negative, flowing from right to left (sinking current), the reverse is true and M2 with R_S become the current limit circuit.

The voltage drops of the bi-directional current limit circuit can be calculated as following:

For positive output ($V_O > 0$, $I_O > 0$),

Equation 2: Positive Voltage Drop of the Bi-Directional Current Limit Circuit

$$V_{DROPTOTAL} = I_O \cdot (R_{DS(ON)M1} + R_S) + V_{DROPD2}$$

For negative output ($V_O < 0$, $I_O < 0$),

Equation 3: Negative Voltage Drop of the Bi-Directional Current Limit Circuit

$$-V_{DROPTOTAL} = -I_O \cdot (R_{DS(ON)M2} + R_S) + V_{DROPD1}$$

The bi-directional current limit circuit will limit both sourcing and sinking output currents at the same amount if the two MOSFETs have the same characteristics ($R_{DS(on)}$, Input Admittance, and etc.).

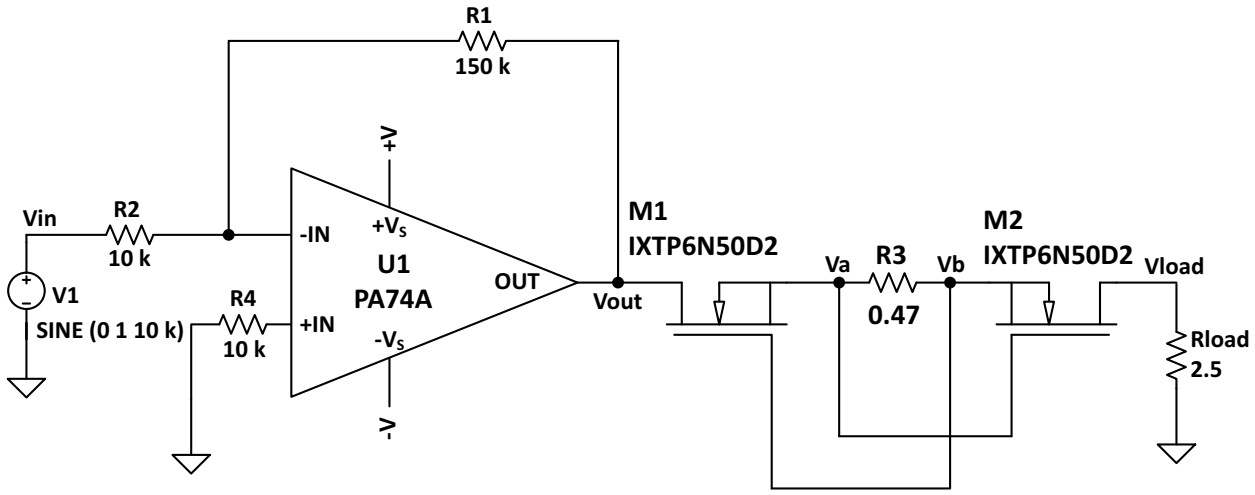
For reactive loads (inductive loads, capacitive loads or both combined), the phase shift of the output voltage and output current will make the system more complicated and should be calculated on a case by case basis.

TEST CIRCUIT FOR EXTERNAL CURRENT LIMIT CIRCUIT AT OUTPUT (OUTSIDE THE CLOSED-LOOP)

CIRCUIT SCHEMATIC AND PART SELECTIONS

The test circuit uses one of the two op amps within an Apex PA74A configured as a basic inverting voltage amplifier and two IXTP6N50D2 for the current limit circuit, as shown in Figure 6.

Figure 6: Bi-Directional Depletion Mode MOSFET Current Limit Circuit at Output (Outside the Closed-Loop)



The PA74A is an Apex 40V dual power op amp with maximum 3A peak output current (within SOA).

The IXTP6N50D2 is a 500V, 6A N-channel Depletion Mode MOSFET made by IXYS Corporation. Table 1 lists some basic characteristics of the device.

Table 1: IXTP6N50D2 Basic Characteristics

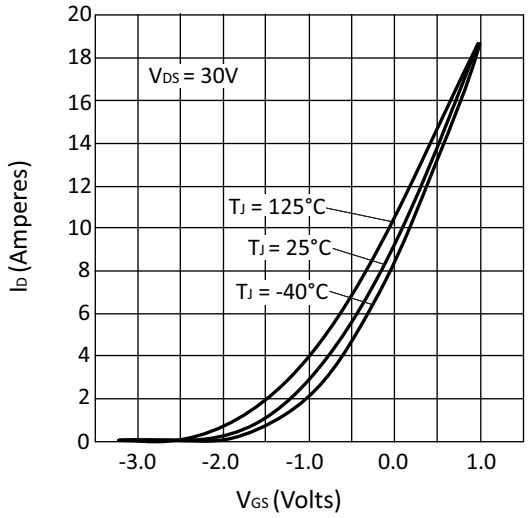
Part No	V_{DSX} (V)	$I_{D(on)}$ (A)	$R_{DS(on)}$ (Ω)	$V_{GS(off)}$ (V)	Package Type
IXTP6N50D2	500	6	0.55	-4.0	TO-220

Figure 7 is the Input Admittance of the IXTP6N50D2. As shown in the graph, when V_{GS} is 0V, the Drain Current I_D is over 8 ampere which is enough for a PA74A application.

To make a current limit circuit with 3A maximum current, the V_{GS} of the MOSFET needs to be about -1V (see Figure 7) which means the current sense resistor should be about 0.33 ohms. The SPICE model provided by the vendor has a slightly different Input Admittance as it requires a 0.47 resistor to limit the current at 3A.

Refer to section 9 Appendix for more details about how to select the MOSFET and current sense resistor R_S.

Figure 7: IXTP6N50D2 Input Admittance



The IXTP6N50D2 has a 15A built-in Source-Drain diode which can be used as the bypassing diode (D1 or D2 in Figure 5). The voltage drop of this diode (V_{SD}) is about 0.8V.

The total voltage loss caused by the current limit circuit can be estimated as $I_O * (R_{DS(on)} + R_S) + V_{DROP} = 3*(0.55 + 0.47) + 0.8 = 3.86V$.

SIMULATION RESULTS

The plots in Figure 8 illustrate the simulation results of the circuit in Figure 6. As discussed in the "External Current Limit Circuit Locations" section, with the current limit circuit located outside the closed-loop, the PA74A's output voltage will not be affected (Figure 8a). The MOSFET starts to limit the output current when VGS is about -1.4V (Figure 8b).

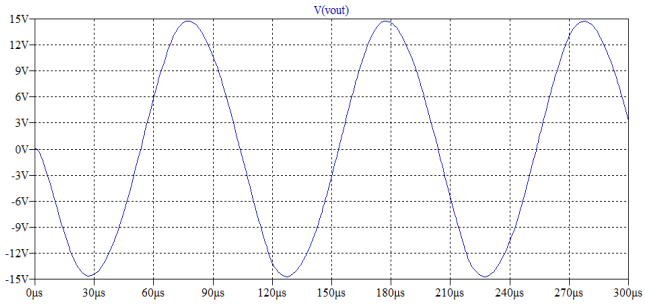
The +/-15V output voltage from the PA74A could drive the 2.5 ohm load up to +/- 6A current, if there is not a current limit circuit. With the external current limit circuit, the voltage delivered to the load is reduced to about 7V (8c) and the load current is limited at about 3A (Figure 8d).

The voltage drop caused by the current limit circuit is not constant because of the current sense resistor. Higher output current will yield more voltage drop. Plots in Figure 8e shows the voltage drops with various loads. In the plot V_{OUT} is the PA74A's output voltage, V_{LOAD} is the voltage delivered to the load and $V_{OUT} - V_{LOAD}$ is the voltage drop caused by the current limit circuit. Figure 8f is the V_{LOAD} with the current limit circuit.

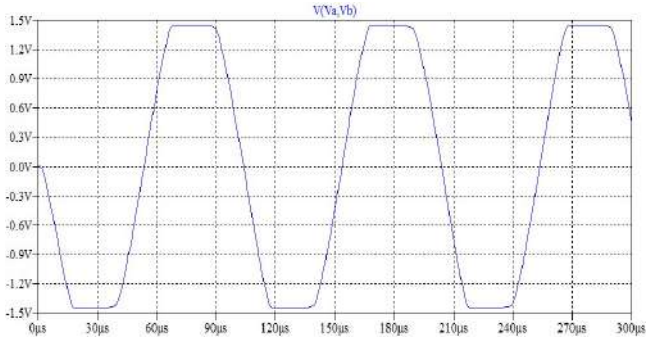
The function of this current limit circuit can be viewed as a non-linear dynamic load for the op amp but will not have an impact to the op amp's closed-loop performance.

Figure 8: Simulation Results for Output Current Limit Circuit at Output (Outside the Closed-Loop)

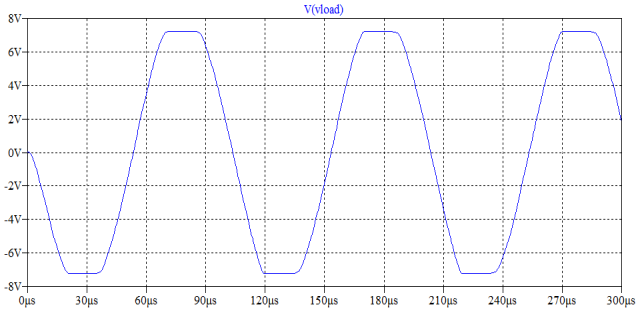
A) PA74A's Output Voltage



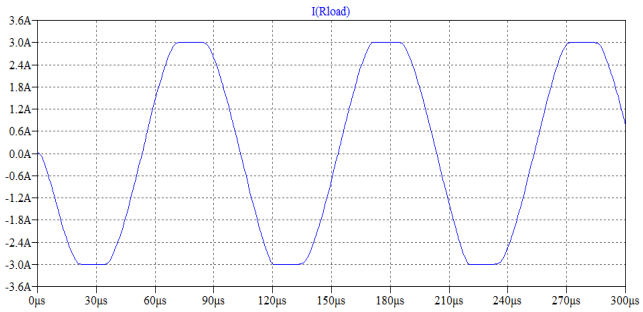
B) V_{GS} (= V_A - V_B in Figure 6)



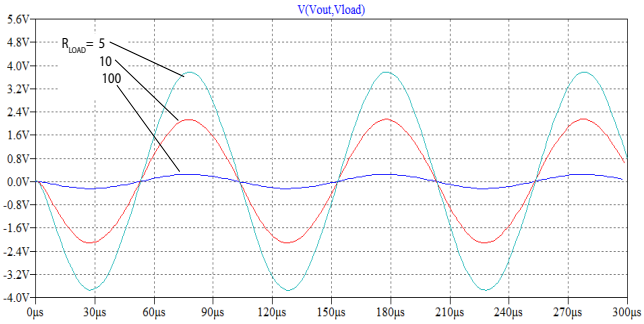
C) Reduced Load Voltage



D) Limited Load Current



E) Output Voltage drop caused by the current limit circuit



F) Load Voltage

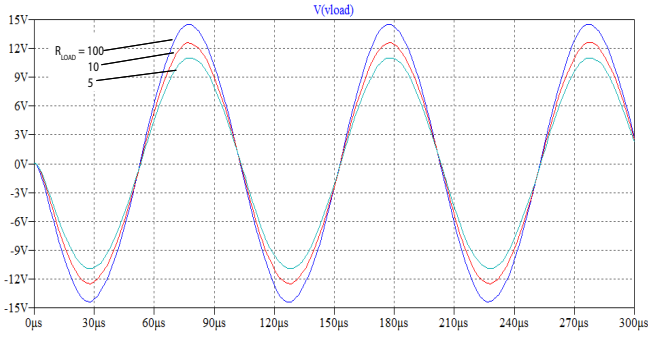
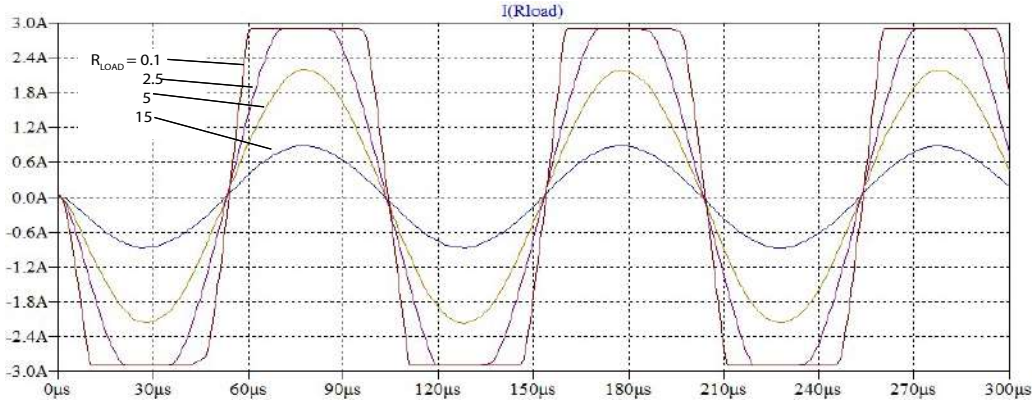


Figure 9 illustrates the simulation results for various load values with same supply voltages and input signal. When the output current is low (R_{LOAD} = 15 ohm or 5 ohm), the current limit circuit is not active. When the load is getting smaller (R_{LOAD} = 2.5 ohm or 0.1 ohm) the load current will increase, per Ohm's Law, and then the current limit circuit becomes active to limit the load current at near 3A maximum.

Figure 9: Output Current with Various Loads



SOA (SAFE OPERATING AREA) ANALYSIS

Figure 10 is the PA74A's SOA graph from the PA74A datasheet, with the load lines of various resistive loads for the circuit using an external current limit circuit. For comparison, Figure 11 is the same SOA/load line graph for the circuit without the current limit function. The load lines in both graphs are from simulation results.

As shown in Figure 10, although the external current limit circuit can limit the maximum output current at 3A for most load conditions, there is still a chance to violate the SOA if the output is shorted to ground. Therefore, a worst case SOA analysis is still a mandatory step in the design process.

Figure 10: PA74A SOA Graph and Various Resistive Load Lines with External Current Limit Circuit

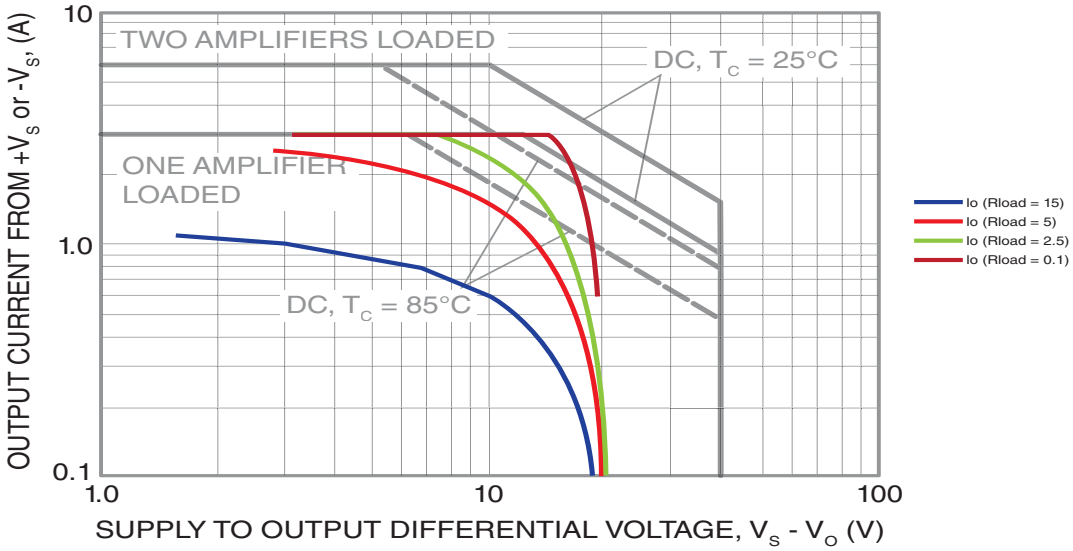
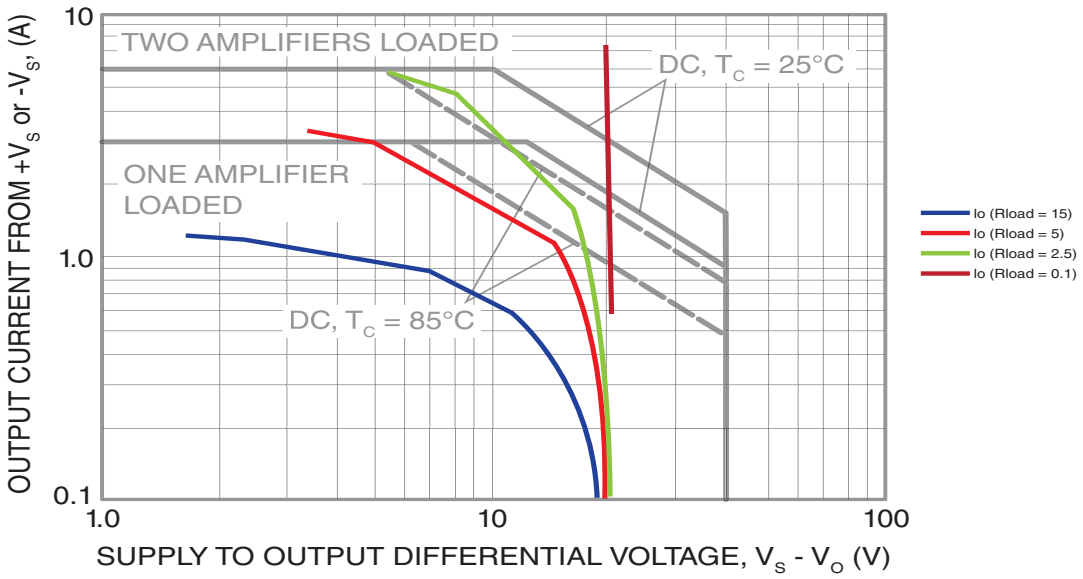


Figure 11: Various Resistive Load Lines with External Current Limit Circuit



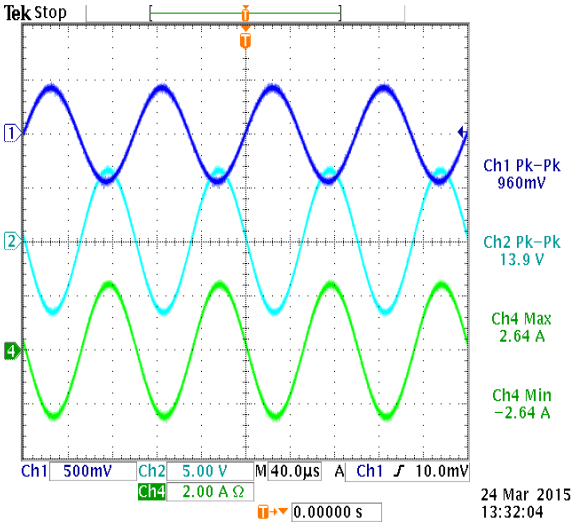
LAB TEST RESULTS

The assembled test board uses the Apex EK21 (Evaluation Kit for PA74/PA74A Pin-Out). This board was configured as an inverting amplifier as shown in Figure 6. Two KIKUSUI PWR800Ms power supply units provide the +/- 20V voltages to the EK board and the 10 kHz input signal is from an Agilent 33522A Waveform Generator. The load is a DALE RH-50 2.5 ohm / 50W resistor with a heat sink. The current sense resistor R3 is a DALE RS-5 0.47 ohm/5W resistor without a heat sink.

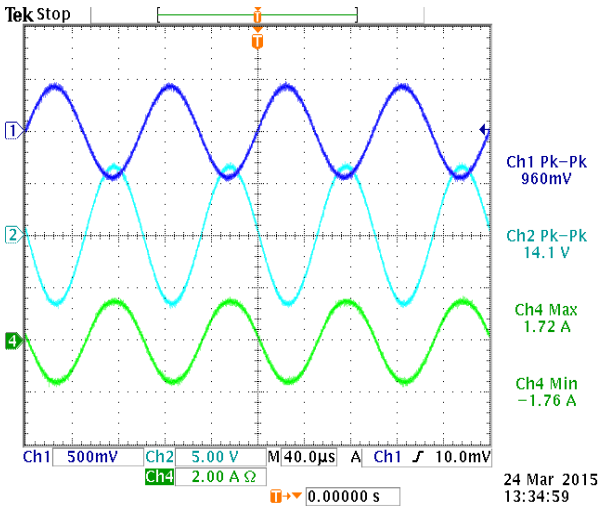
Oscilloscope captures in Figure 12 show the lab test results (Ch1: PA74A's Input Voltage, CH2: PA74A's Output Voltage, CH4: Load Current). Before adding the current limit circuit to the system, the peak output current of the system is about 2.6A when the input is 960mV (Figure 12a). After adding the current limit circuit, with the op amp's output voltage kept the same (about 14V), the load current is limited at 1.7A without clipping (Figure 12b). With even higher output voltage (about 25V), the output current is clipped at about 2.2A (Figure 12c).

Figure 12: Lab Test Results for Current Limit Circuit at Output (Outside the Closed-Loop)

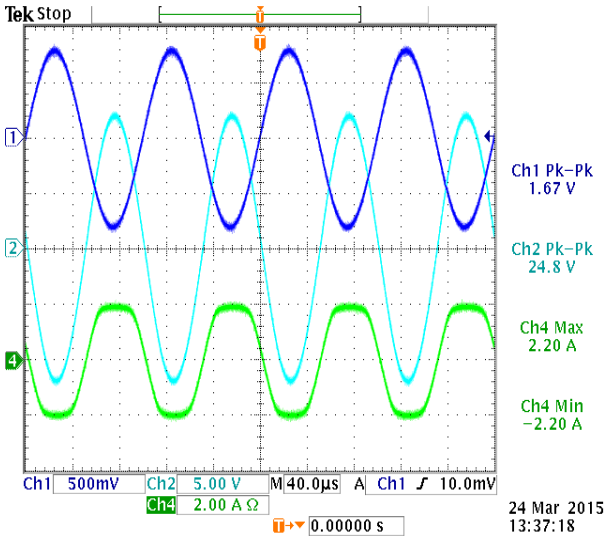
A) Before adding the current limit circuit



B) After adding the current limit circuit



C) Output Current clipped by the current limit circuit

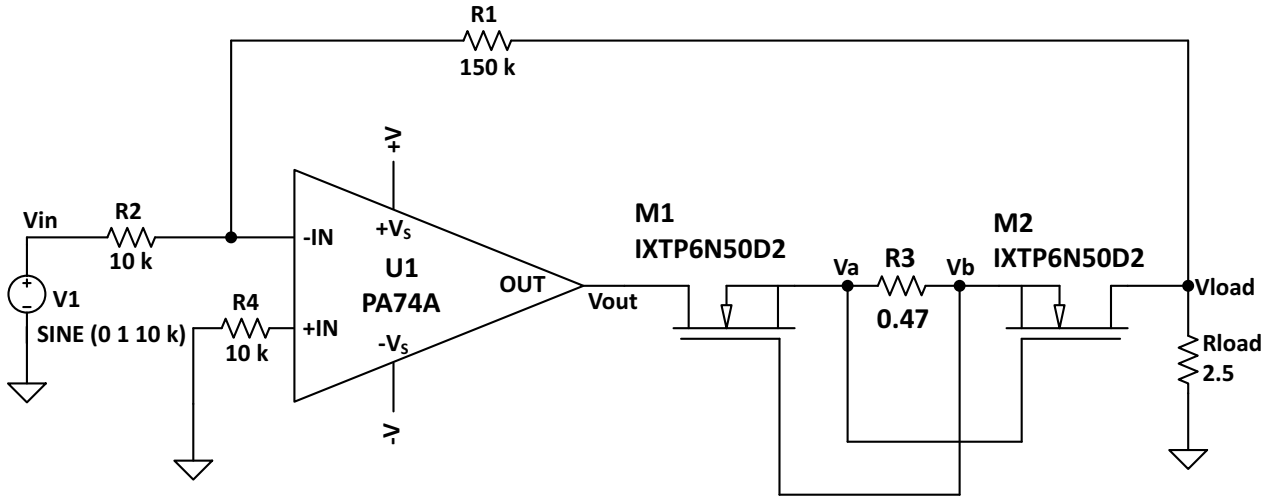


TEST CIRCUIT FOR EXTERNAL CURRENT LIMIT CIRCUIT AT OUTPUT PATH (INSIDE THE CLOSED-LOOP)

CIRCUIT SCHEMATIC

The test circuit uses the same Apex PA74A, with the PA74A's feedback resistor connected to the load, as shown in Figure 13.

Figure 13: Bi-Directional Depletion Mode MOSFET Current Limit Circuit at Output (Inside the Closed-Loop)



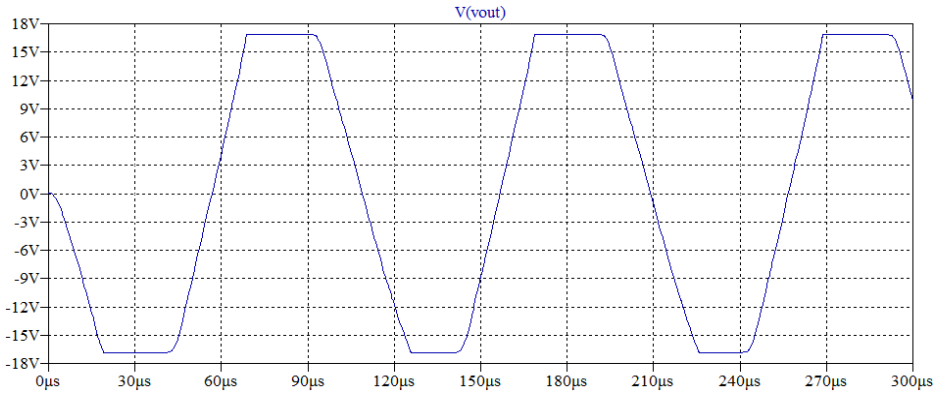
SIMULATION RESULTS

The plots in Figure 14 illustrate the simulation results of the circuit in Figure 13. As discussed in the "External Current Limit Circuit Locations" section, with the current limit circuit located inside the closed-loop, the PA74A's output voltage will be affected. With the same 2.5 ohm load, the PA74A's output voltage is limited at about 17V maximum (Figure 14a). The MOSFET starts to limit the current when V_{GS} is about -1.4V (Figure 14b), same as the system with the current limit circuit outside the closed-loop.

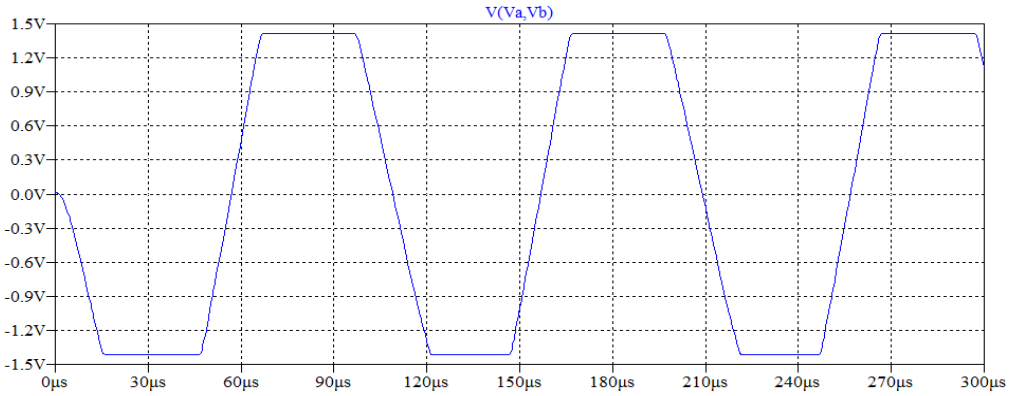
The voltage delivered to the load is shown in Figure 14c and the load current is limited at about 2.9A (Figure 14d). Figure 14e illustrates the voltages delivered to the load, with different load resistances.

Figure 14: Simulation Results for Output Current Limit Circuit at Output (Inside the Closed-Loop)

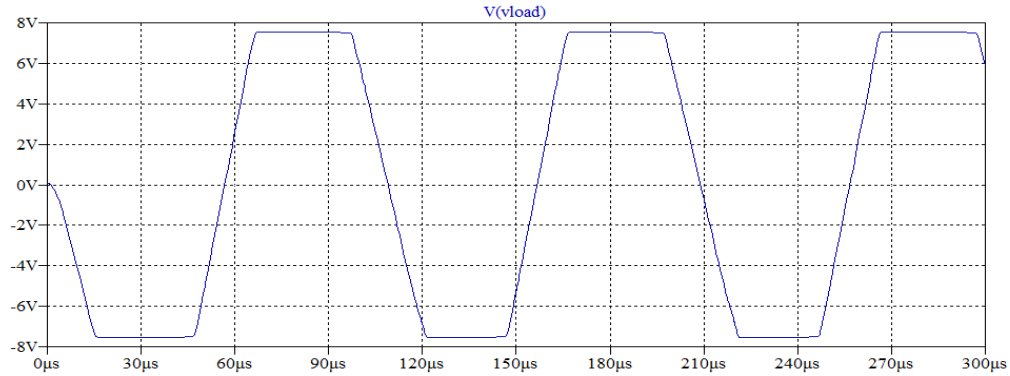
A) Reduced PA74A's Output Voltage



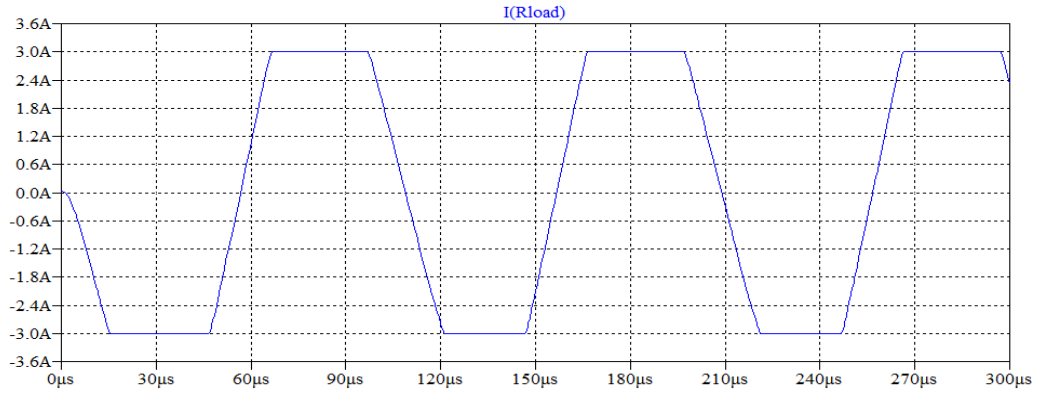
B) V_{GS} (=V_A - V_B)



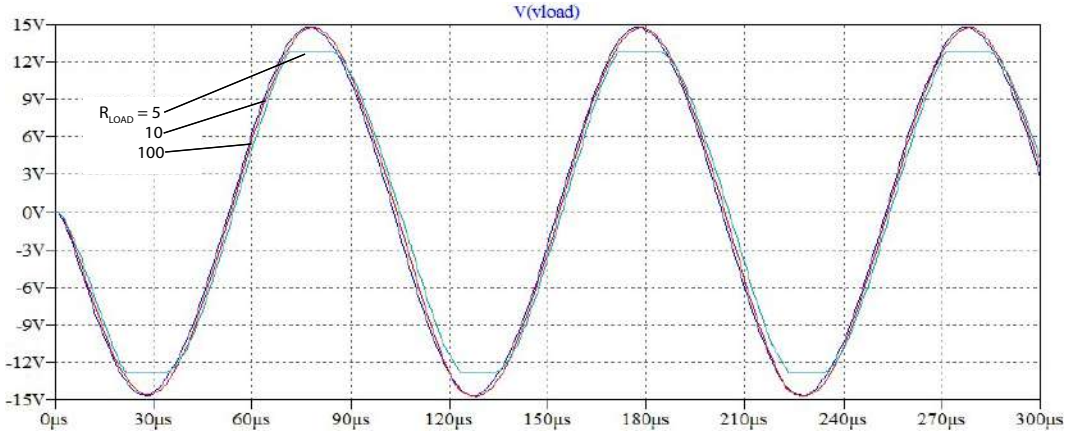
C) Load Voltage



D) Limited Load Current

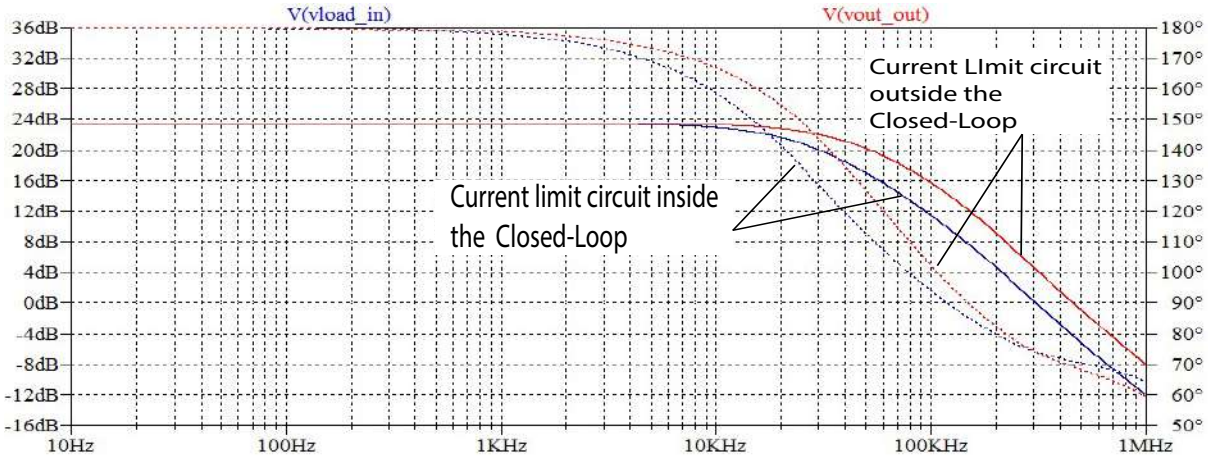


E) Load Voltage



The current limit circuit inside the closed-loop could add additional output delay to the system. Figure 15 compares the gain and phase differences with the current limit circuit placed at the two different locations. Reduced phase margin and lower voltage gain can be found when the current limit circuit is placed inside the closed-loop.

Figure 15: Closed-Loop Gain and Phase Responses for Two Current Limit Circuit Locations



SOA ANALYSIS

The load lines for this configuration are the same as those in since V_O, I_O and R_{LOAD} are not changed. Therefore, a worst case SOA analysis is also required in the design process.

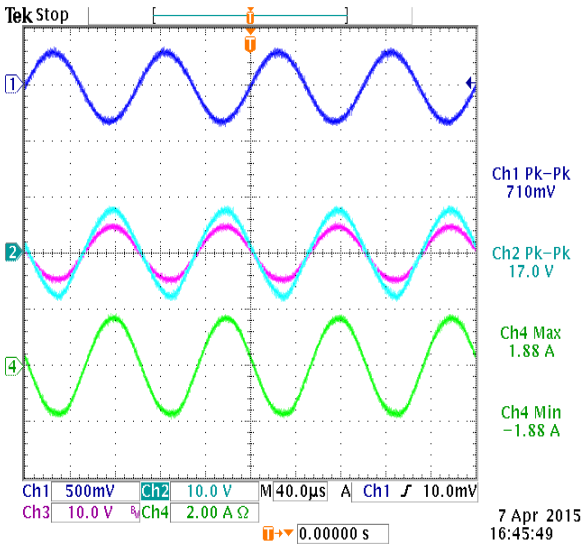
LAB TEST RESULTS

The test board uses the same EK21 with modifications to put the current limit circuit inside the closed-loop, as shown in Figure 13.

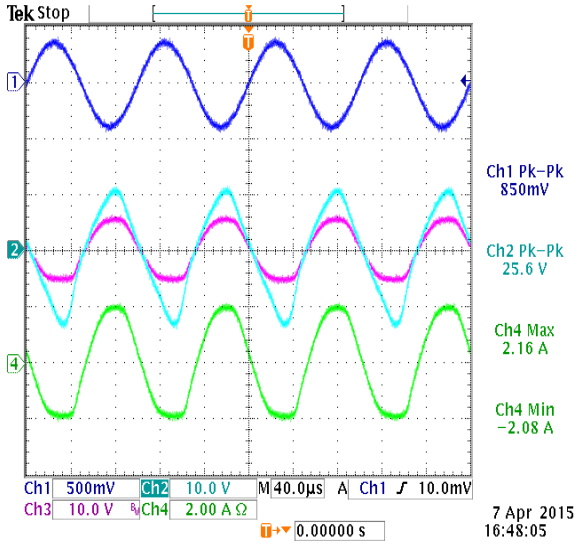
When the output current is less than 2A, the current limit circuit is inactive (Figure 16a). The maximum output current is about 2.2A allowed by the current limit circuit (Figure 16b and 16c). Channel 3 (pink) in the captures is the voltage delivered to the 2.5 ohm load, which is also the feedback voltage of the closed-loop.

Figure 16: Test Results for Output Current Limit Circuit Inside the Closed-Loop

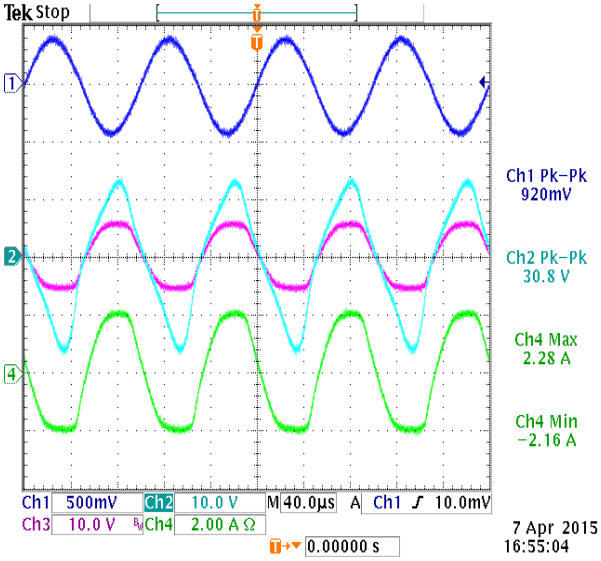
A) Io = 2A, no current limiting



B) The maximum output current is limited to 2.2A



C) Higher output voltage will not effect the max current

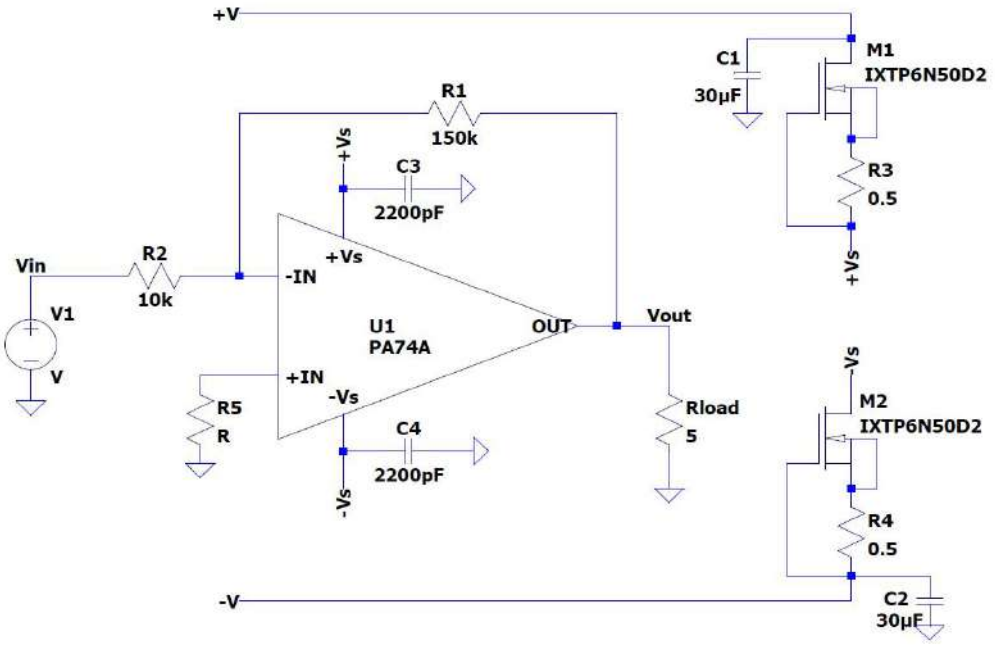


TEST CIRCUIT FOR EXTERNAL CURRENT LIMIT CIRCUIT AT THE POWER SUPPLY RAILS

CIRCUIT SCHEMATIC

The test circuit uses the same Apex PA74A configured as an inverting voltage amplifier. Two IXTP6N50D2 circuits are connected at the op amps power pins as shown in Figure 17.

Figure 17: Test Circuit for Current Limit Circuit at Power Supply Rails

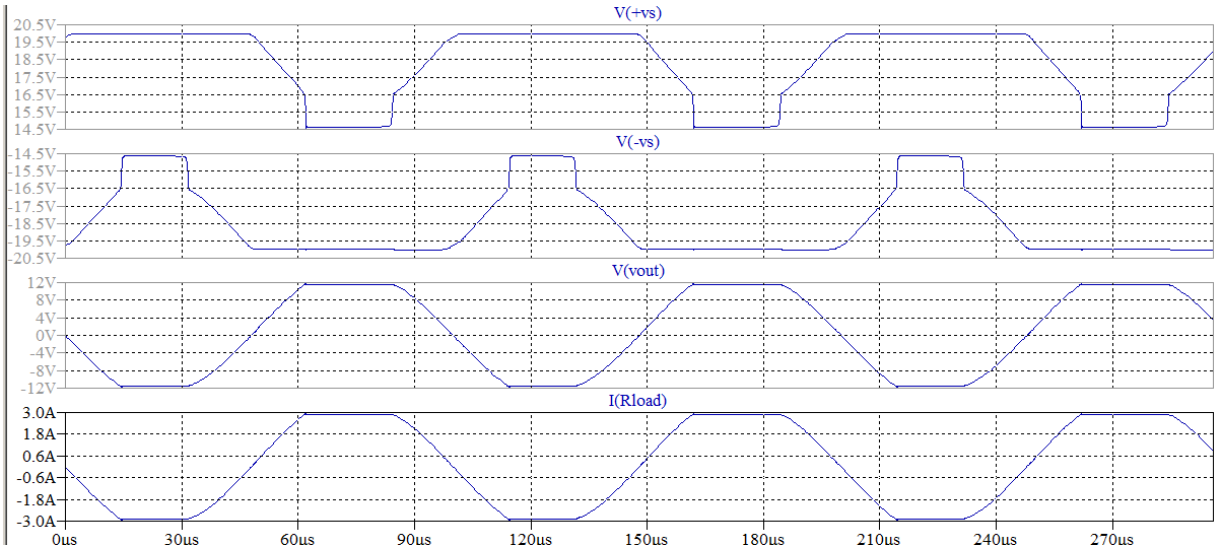


Bulk capacitors (C1 and C2 in Figure 17) are recommended for all Apex power op amps (minimal 10uF per ampere of output current) and must be connected at the supply rails, not at the +/- Vs pins of the op amp like in typical applications.

SIMULATION RESULTS

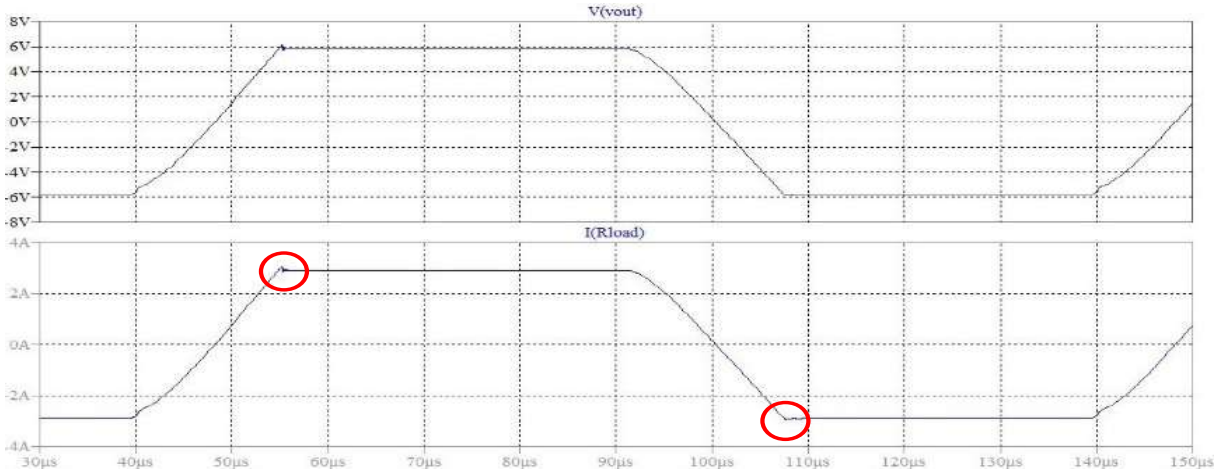
The waveforms in Figure 18 illustrate the simulation results of the power supply rail current limit circuit. The current limit circuit will change the voltages delivered to the op amp, like an envelope tracking power supply. Therefore, the output voltage of the op amp will also be changed when the current limit circuit is active.

Figure 18: Simulation Results for Supply Rail Current Limit Circuits



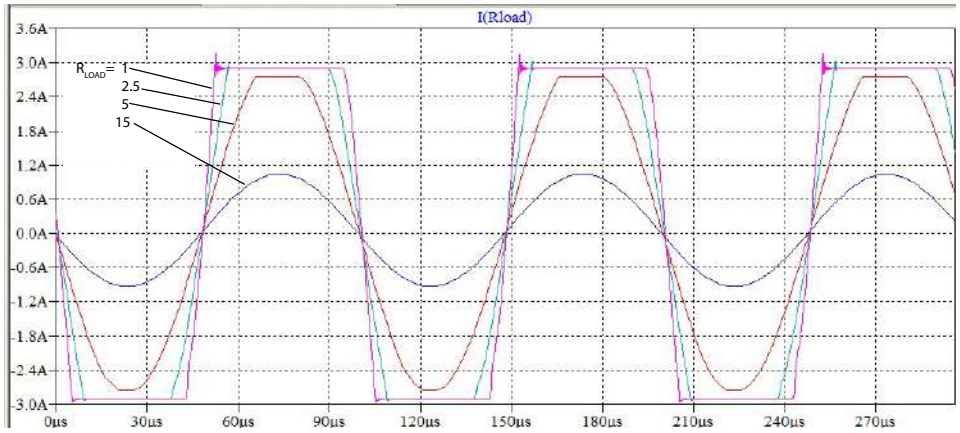
Since this current limit circuit will change the supply voltages, the value of the high frequency bypassing capacitors (C3 and C4 in Figure 17) will affect the current limiting performance. Larger capacitors will increase the response time of the current limit function. This could cause some output overshoot and/or undershoot (see Figure 19). On the other hand, if the capacitors are too small, they may not be able to efficiently filter out the high frequency noises.

Figure 19: Overshoots caused by the High Frequency Bypass Caps



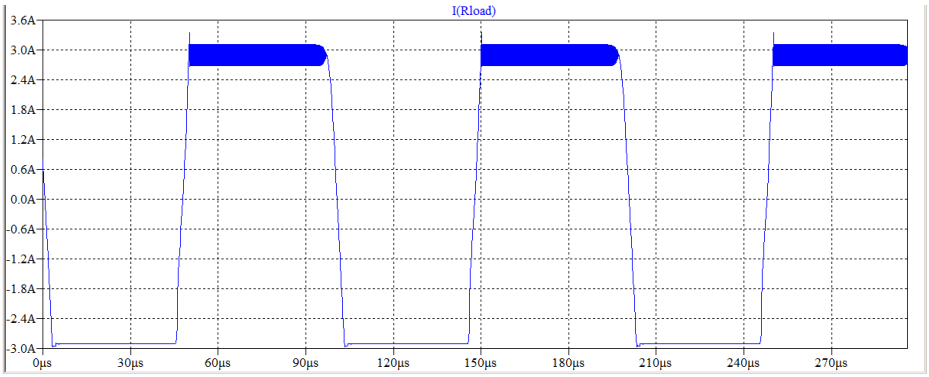
Another issue with the supply rail current limit circuit is the possibility of oscillation when the load is very small. Figure 20 illustrates the simulation results with R_{LOAD} = 1, 2.5, 5 and 15 ohms. When the load is 1 ohm, overshoot with longer settling time can be seen at the positive side of the output current.

Figure 20: Simulation Results for Supply Rail Current Limit Circuits with Various Loads



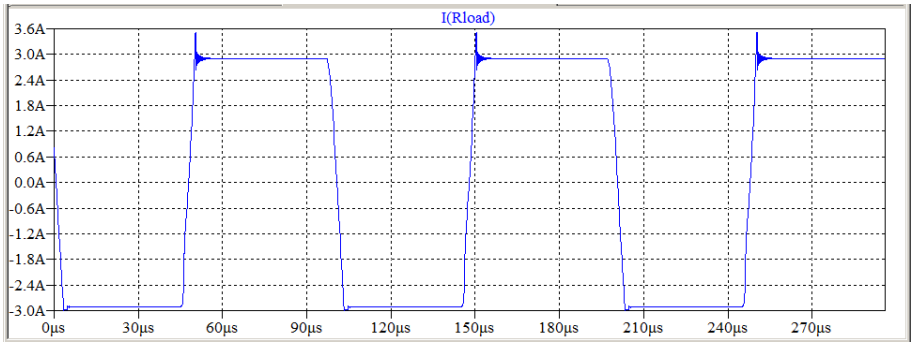
With an even smaller load like 0.1 ohm (near short circuit), the settling time becomes much longer and could lead to an oscillation, as shown in Figure 21.

Figure 21: Simulation Results for Supply Rail Current Limit Circuits with 0.1Ω Load



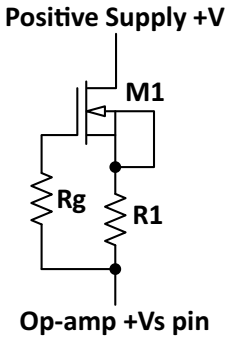
Increasing the high frequency bypass capacitor's value can reduce the settling time but will cause some level of overshoot. Figure 22 illustrates the simulation result with 6200 pF capacitors. The output current has about 0.6A of overshoot.

Figure 22: Output Oscillation Fix with the Cost of Overshoot



Another method to fix the oscillation issue is to add a small resistor R_G as shown in Figure 23.

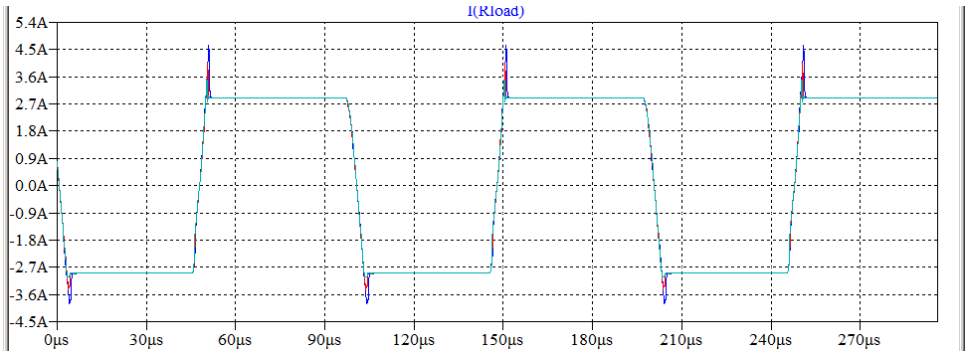
Figure 23: Output Oscillation Fix by adding a small Resistor, R_G



This fix has a similar result as using larger high frequency bypassing capacitor. It will reduce the settling time and stop the oscillation, but at the cost of some overshoots and/or undershoots. Figure 24 illustrates the simulation results for R_G = 10 ohm, 5 ohm and 1 ohm, with the output current overshoot at about 1.73A, 1.1A and 0.5A respectively. The negative side undershoots are smaller. This is due to the circuit difference of the op amp's positive and negative output stages.

Figure 24: R_G Caused Overshoots

A) Output Current overshoots caused by R_G



B) Zoom-In of the overshoots

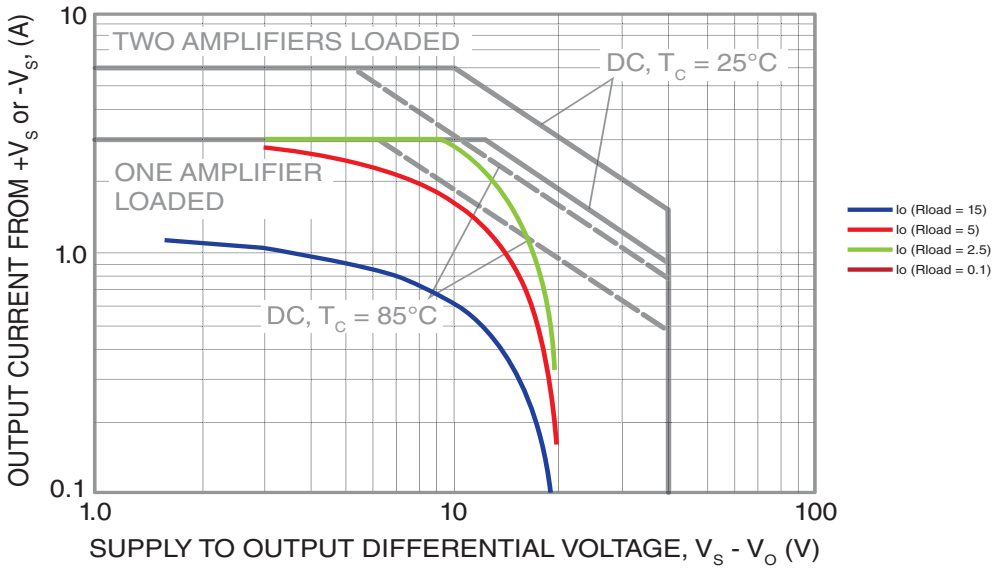
Since most simulation models are first order approximations, the simulation results can be different from the real circuit. Therefore, the recommendation is to experiment with the real circuit to determine the best R_G value.

SOA ANALYSIS

The load lines for this configuration are shown in Figure 25. For the 0.1 ohm load, since the current limit reduces the supply voltage down to 0.3V to get the 3A output current, the load line becomes a single point (0.3V, 3A) on the SOA graph.

It is clear that for all tested load values, the load lines are within the device SOA. It will be an advantage for applications that need to protect the output short to ground.

Figure 25: Load lines for Rail Current limit Circuit



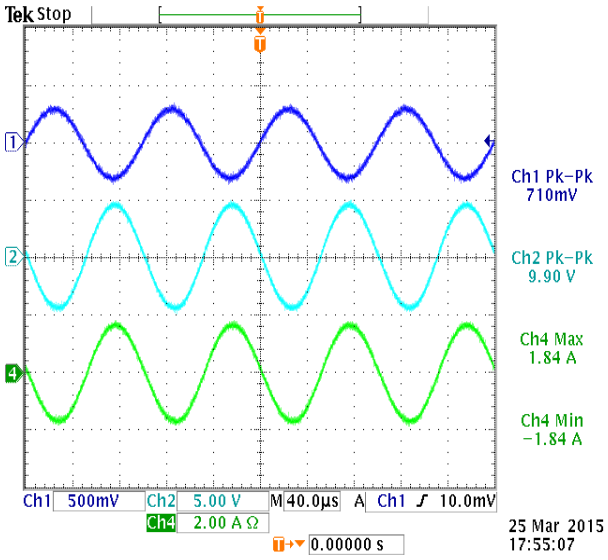
LAB TEST RESULTS

The same EK21 with the same inverting amplifier configuration as described in the “Test Circuit for External Current limit circuit at Output (outside the closed-loop)” section, plus current limit circuits at the supply lines were used to create the test circuit as shown in Figure 17. The 30uF bulk capacitors on the EK21 were moved to the supply rail side of the current limit circuits.

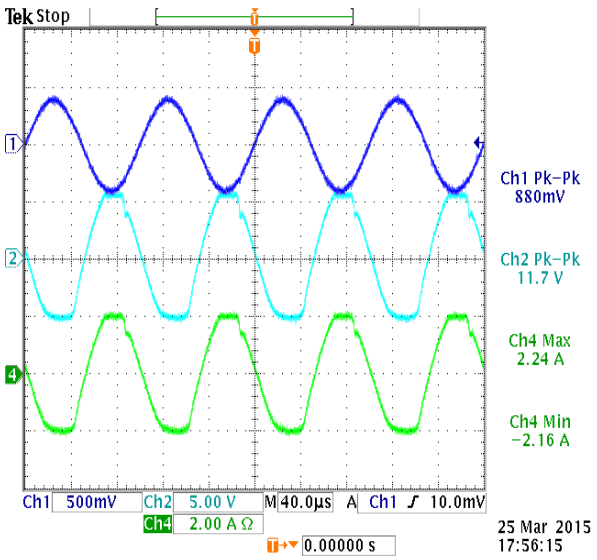
Oscilloscope waveform captures in Figure 26 show the lab test results of the supply rail current limit circuit (Ch1: PA74A’s Input Voltage, CH2: PA74A’s Output Voltage, CH4: Load Current). Waveform (26a) is the result with a small input signal and the output current is about +/- 1.8A which is less than the current limit circuit’s threshold. Waveform (26b) is the result with a higher output current and the external current limit circuits at the power supply rails are active. Waveform (26c) has further current limiting and the waveform (26d) is the result with the op amp’s output shorted to ground. The maximum current allowed by the current limit circuit is about 2.4A. Please note that the 3.7V peak-to-peak output voltage in 26d is the switching noise caused by the current limit circuit, not the real output voltage since with near 0 ohm load the output voltage should be around zero as well.

Figure 26: Lab Test Results for Supply Rail Current Limit Circuit

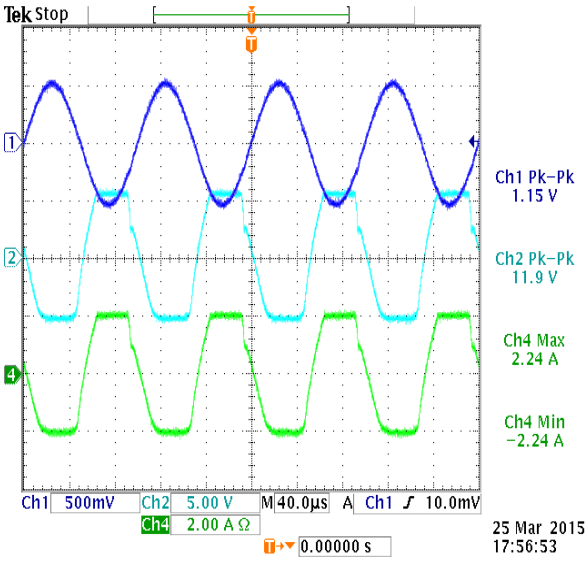
A) No current limiting at I_O = 1.8A



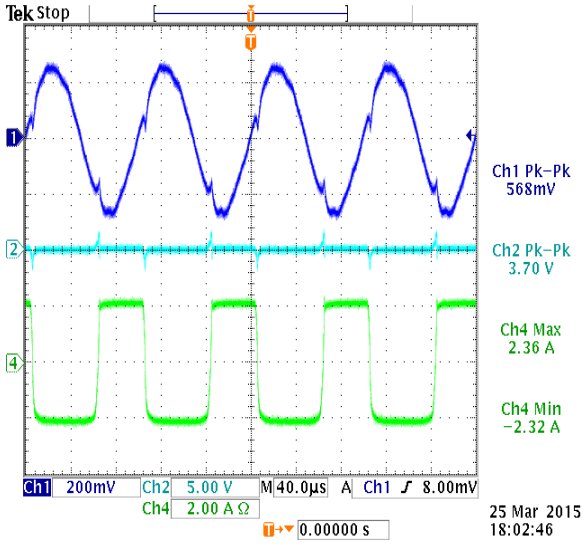
B) Current Limit Circuit starts to be active



C) Further Limiting



D) Load is near zero



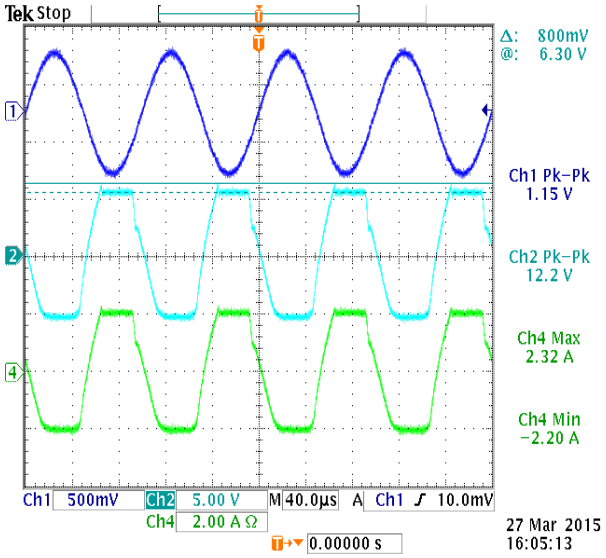
The capture (c) and (d) in Figure 26 have some notable glitches on the falling edge of each cycle. The glitches in capture (d) even affected the input signal (due to the low driving capability of the signal generator) through the feedback path. This is due to the fast switching speed of the MOSFET with high current load. If

this becomes a concern for the application, a small resistor R_G (same as the one shown in Figure 23) can be added to fix the issue.

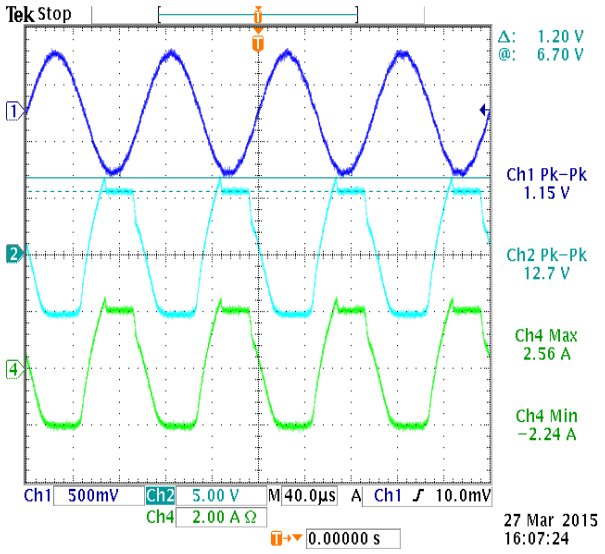
The value of the R_G depends on the characteristics of the MOSFET. A larger R_G can work better for smoothing the glitch but on the other hand it can cause overshoot on the rising edge. Oscilloscope waveform captures in Figure 27 show the lab test results with R_G = 10, 50, 75 and 150, and the overshoot voltages for these resistor values are about 0.8V, 1.2V, 1.3V and 1.8V respectively.

Figure 27: Lab Test Results with Various R_G Values

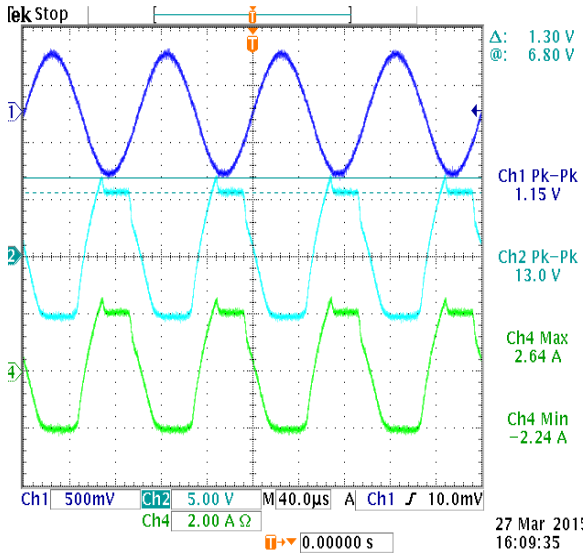
A) R_G = 10



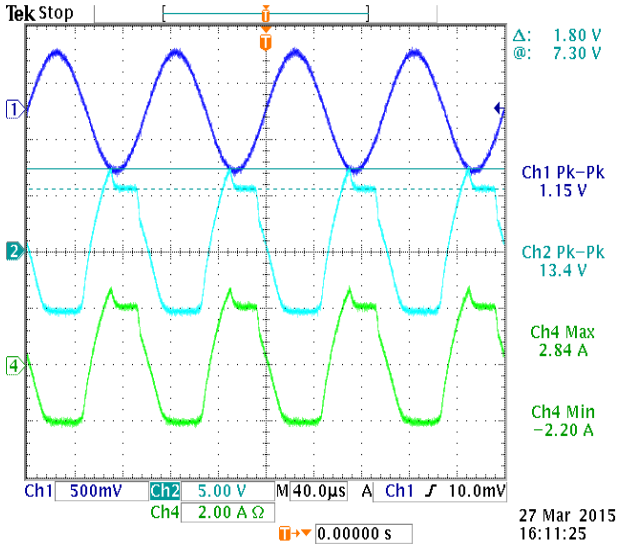
B) R_G = 50



C) R_G = 75



D) R_G = 150



It must be made clear that any current limit circuit discussed in this article uses the non-linear characteristics of the MOSFETs. Therefore, in general once the current limit circuit is active, output distortions (like clipping, glitch, and etc.) cannot be avoided.

Note: Output oscillations discussed in the "Simulation Results" section were not observed in the lab tests. One possible reason is due to the differences between the simulation model and the real devices. It is also possible that the parasitic capacitance on the board added more stability to the system.

BEST PRACTICES FOR BUILDING AN EXTERNAL CURRENT LIMIT CIRCUIT

- The MOSFETs will need a heat sink and the design (power, current and temperature) must follow the SOA specifications for the MOSFETs.
- Many high power MOSFETs have the heat tab/slug tied to the Drain or Source. Therefore, two of these MOSFETs cannot share the same heat sink, unless they are electrically isolated from the heat sink.
- Current sense resistors consume power, and may require heat sinks.

APPENDIX

STEPS TO SELECT THE DEPLETION MODE MOSFETS AND THE CURRENT SENSE RESISTOR

Step 1: Find a MOSFET with voltage and current ratings meeting the application's requirements.

Step 2: Verify the on-resistance of the MOSFET is low so the voltage drop(s) caused by the MOSFET(s) will be acceptable for the application.

Step 3: Verify the Drain current (I_D) of the MOSFET is larger than the desired current limiting value, when the Gate voltage V_{GS} is zero. In general, a device with Input Admittance characteristics as shown in Figure 28 cannot be used since its I_D is too small when V_{GS} is zero, and the simple design discussed in this article cannot provide a positive V_{GS} to the MOSFET.

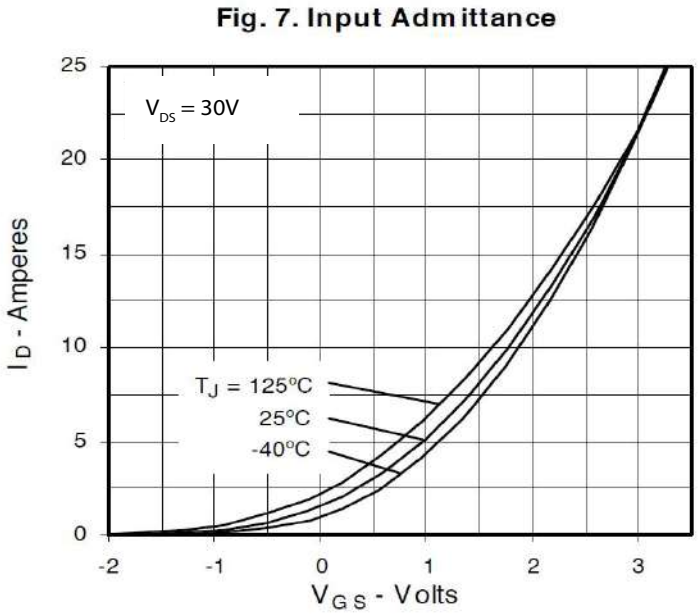
Step 4: Estimate the value of the current sense resistor R_S ($R_S = V_{GS1}/I_{ILIMIT}$, where the I_{ILIMIT} is the desired maximum current of the application and V_{GS1} is the Gate-Source voltage of the MOSFET at $I_D = I_{ILIMIT}$).

Step 5: Run a simulation if the MOSFET's SPICE model is available. Due to the non-linear characteristic of the input admittance and variations among MOSFETs, it could be necessary to adjust the calculated R_S value, and a simulation will be very helpful.

Step 6: Determine the power rating of current sense resistor R_S and select the right heat sinks for the R_S and the MOSFETs.

Step 7: Build a prototype circuit to test the current limit function and adjust the R_S value if necessary.

Figure 28: A MOSFET Unsuitable for Current Limit Circuit



The typical value of the current sense resistor R_S is 0.1~ 1 ohm. If R_S is too big, it will have a high voltage drop and increase the power consumption. Since the correlation of a MOSFET's I_D and V_{GS} is not linear (see Figure 28), sometimes the value of the current sense resistor may not be easily determined by calculations or even simulations. On the other hand, the tolerance of the components used in the circuit could also affect the accuracy of the current limit circuit. Therefore, for most applications, bench testing could be the only method to find the correct R_S value.

A MOSFET's characteristics (I_D, $R_{DS(on)}$, Input Admittance, etc.) could also be affected by the temperature of its working environment and should be considered if the application needs to work at various temperature conditions.

It is important to remember that the objective of using current limit circuits (either built-in or external) is to protect the op amp at some unusual conditions. The current limit circuits discussed in this article and Apex AN09 should never be used as precision output current controllers, since the current limited by those circuits could have +/-20% variations.

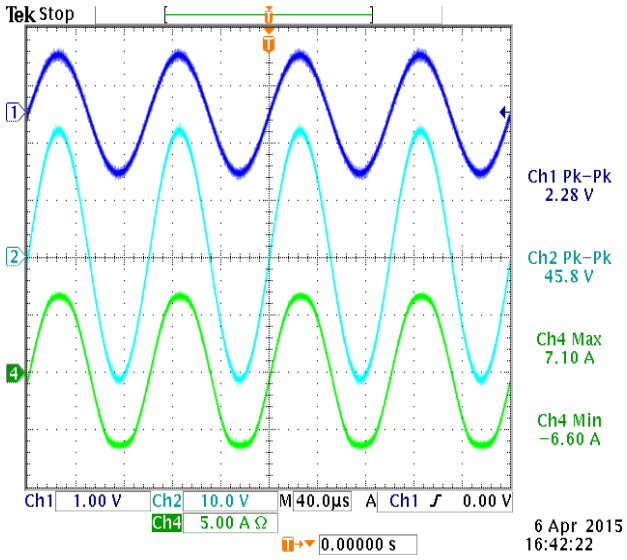
EXTERNAL CURRENT LIMIT CIRCUIT FOR SUPER HIGH CURRENT OP AMPS

The external current limit circuits discussed in previous sections also can be used for super high current op amps like PA50 (100V, 100A peak) or PA52 (200V, 80A peak). However, trying to find Depletion Mode MOSFETs with such high current ratings might be difficult. Moreover, component-to-component tolerances seems to be playing an increasing role when the current requirement goes up, resulting in asymmetric current limiting behavior.

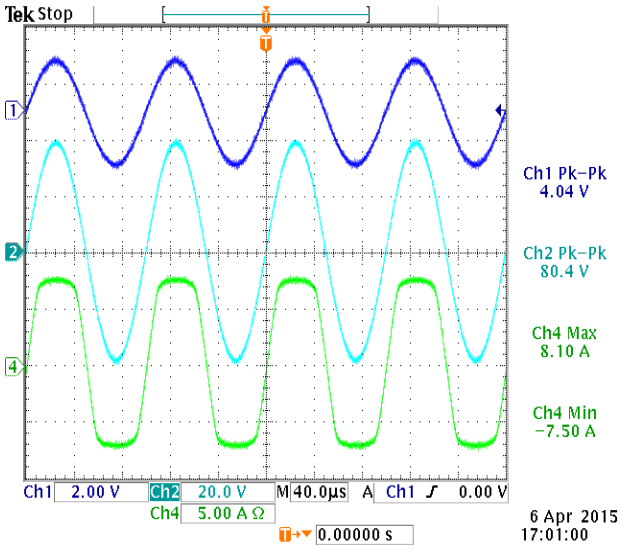
An IXTH16N20D2 (200V, 16A, 80mohm) based external current limit circuit, same as the one shown in Figure 6 but with a 0.12 ohm current resistor, has been tested for Apex PA52, using Apex EK29 Rev. B board. The test results are shown in Figure 29.

Figure 29: Lab Results of an 8A External Current Limit Circuit

A) Current Limiting Begins at about 6.6A ~ 7A

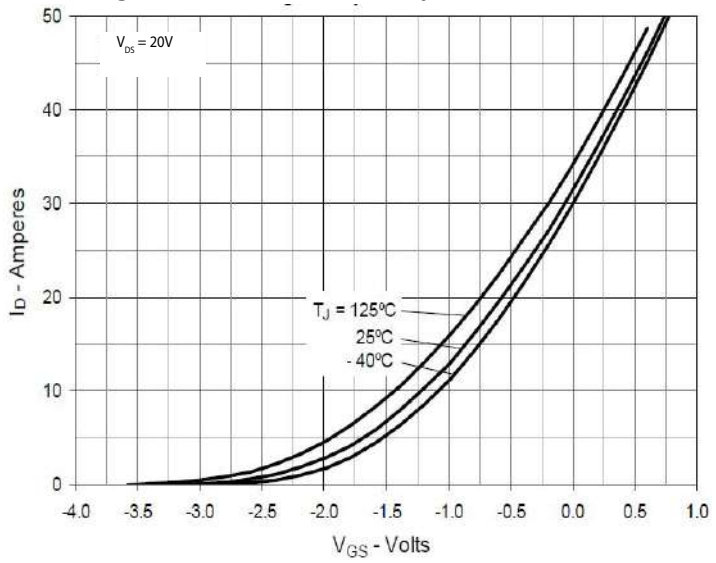


B) The Maximum Output Current is about 7.5A ~ 8A



The maximum output current is about 8A for the tested circuit, nearly 20% less than the typical performance specified in the IXTH16N20D2 datasheet (Figure 30). Also the positive and negative currents were limited at different levels and the cause is the variations of the two MOSFETs used in the circuit (Switching the connections of the equivalent 2-terminal current limit circuit, in connect the op amp's output to the right side of the current limit circuit and connect the load to the left side of the current limit circuit, will yield the opposite results as shown in Figure 29).

Figure 30: IXTH16N20D2 Input Admittance



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- 16N20D2 Data Sheet, IXYS Corporation (http://ixapps.ixys.com/DataSheet/DS100260C%28IXTH-T16N20D2%29.pdf)